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Change list	
A1	1. Add 2x10 male JTAG header J12 for zigbe module 2. Separate CT pins of magnetic U1/U2 to save several mA current 3. Change MPC8308 pin Y23 from NC to VDD (net VCORE) per latest MPC8308EC Rev 2 4. Remove DNP pull up resistors R42/R43 on net MDIO 5. EMI consideration 1) Change R140 from DNP to populate 2) Change C75/C78/C80/C93 from DNP to populate 3) Change C121/C122 decoupling capacitors for PHY VDDH from 0.1uF to 100pF 4) Add 18pF capacitors C359/C360 to GND on net TSEC1_GTX_CLK25 & TSEC2_GTX_CLK25 5) Change terminated series resistors R36/R37 on net G1_RX_CLK & G2_RX_CLK from 0ohm to 22ohm, add series bead L32/L31 and 18pF capacitors C363/C362 to GND 6) Add series bead L30/L31 and 18pF capacitors C361/C362 to GND on net G1_GTX_CLK & G2_GTX_CLK 7) Add bead L34/L35 on U6/U7 pin3 VDD33 8) Swap MDI interface on magnetic U1/U2 6. Remove test point TP1~TP2, TP6~TP8, TP10~TP16, TP21, TP22, TP18 for layout space limitation

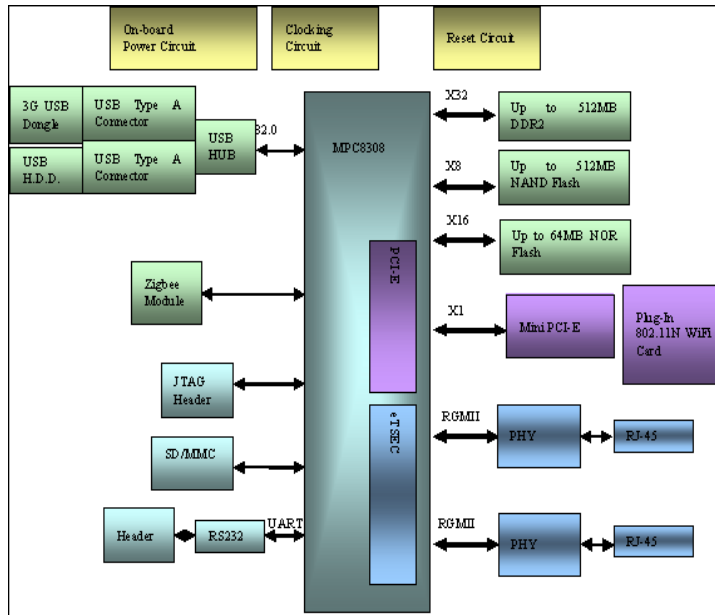
Revisions			
Rev	Description	Date	Approved
A	Release Rev. A	April 6,11	
A1	Add 2X10 JTAG Header for Zigbee Module Changes for EMI consideration. Details refer to A1 change list.	June 24,11	
B	Release Rev. B	June 30,11	

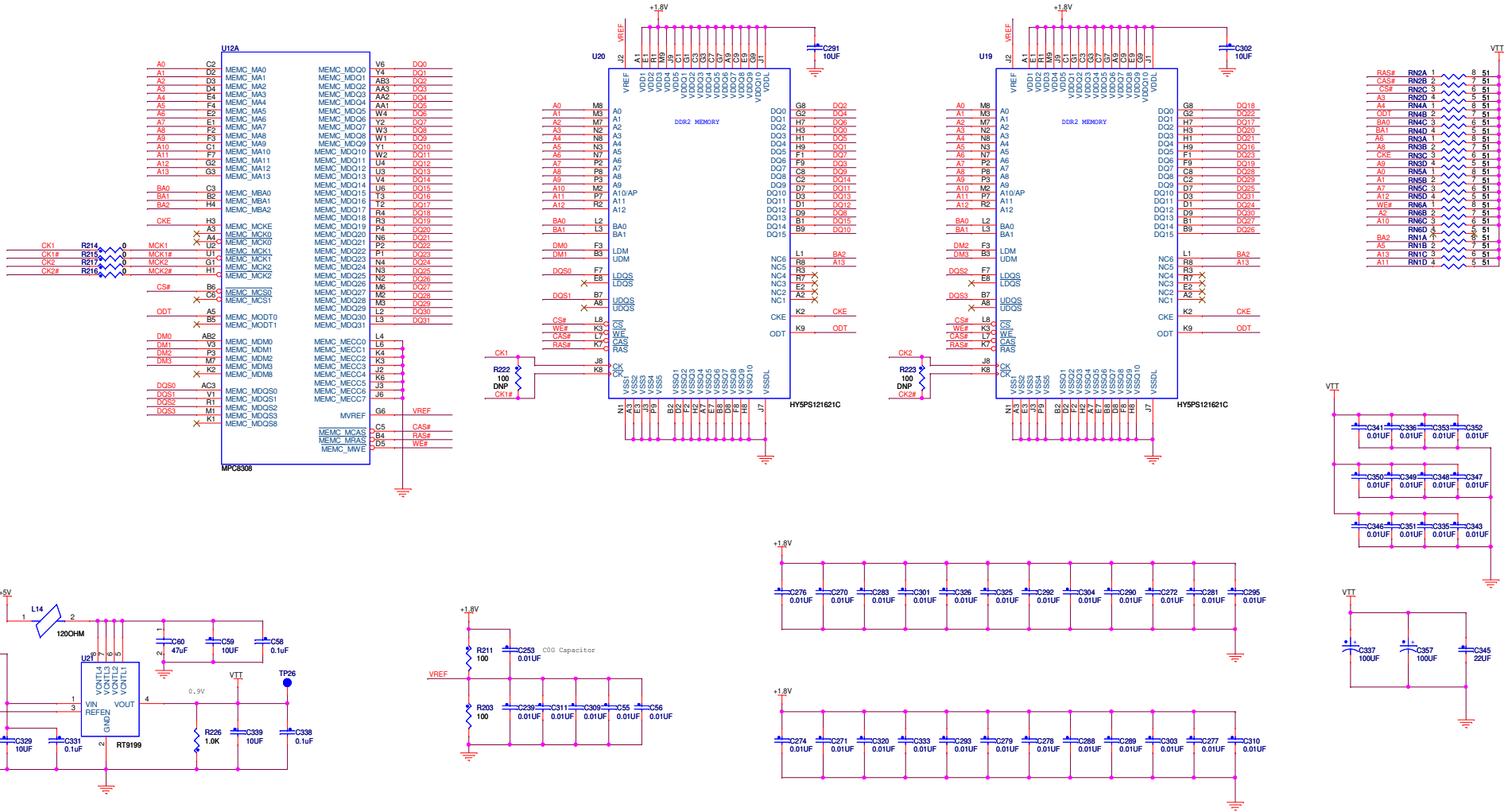
MPC8308 - NSG

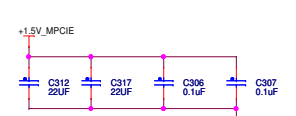
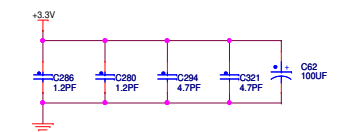
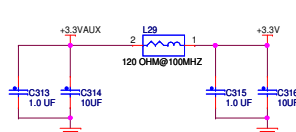
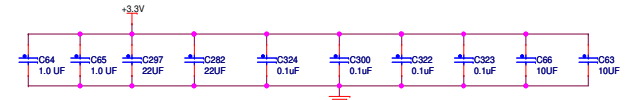
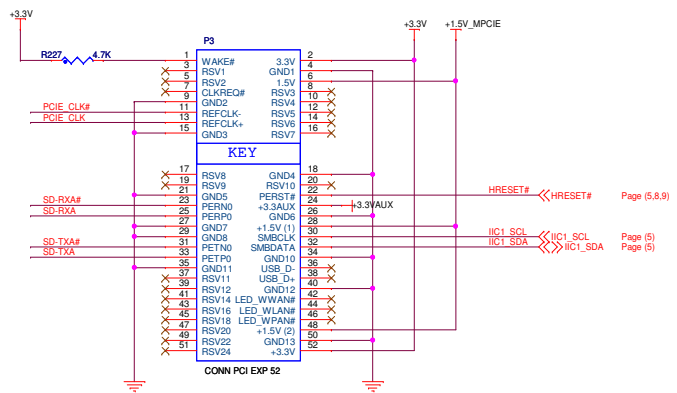
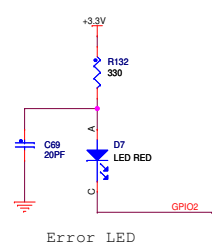
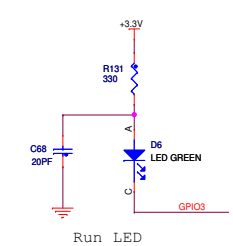
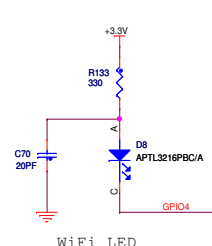
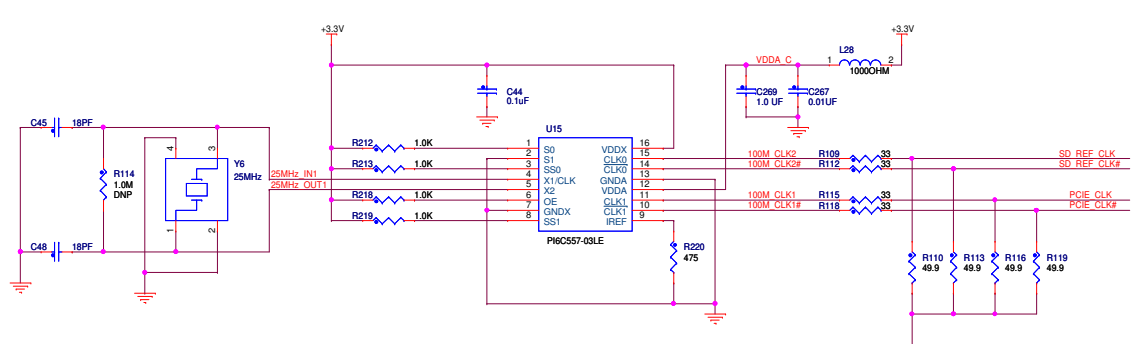
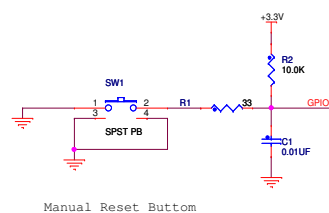
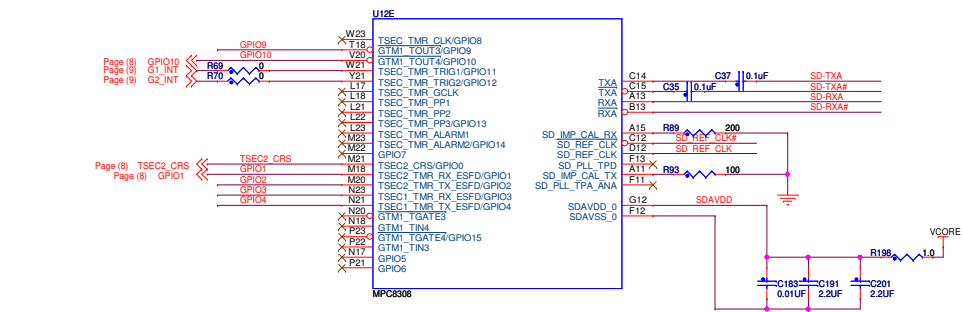
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Designer: James Zhang		ICAP Classification: FQP: FIUQ: X PUB:	
Drawn by: James Zhang		MPC8308 - NSG	
TITLE PAGE			
Approved: Taris Qiu	Size C	Document Number SCH-27072 PDF: SPF-27072	Rev B
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1. Unless Otherwise Specified:
All resistors are in ohms
All voltages are DC
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

		
ICAP Classification: FCP: FIUC: X PUBI: _____		
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Page Title: NOTES		
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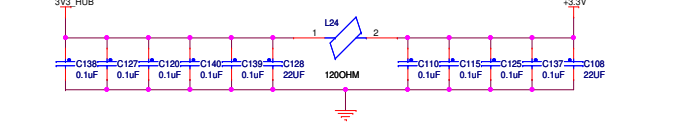
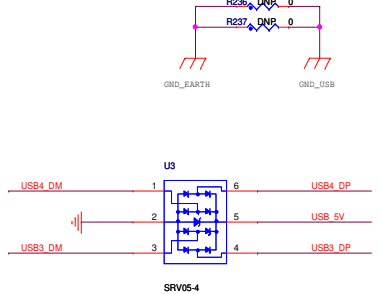
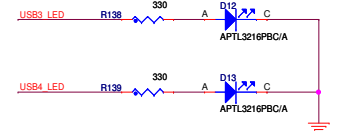
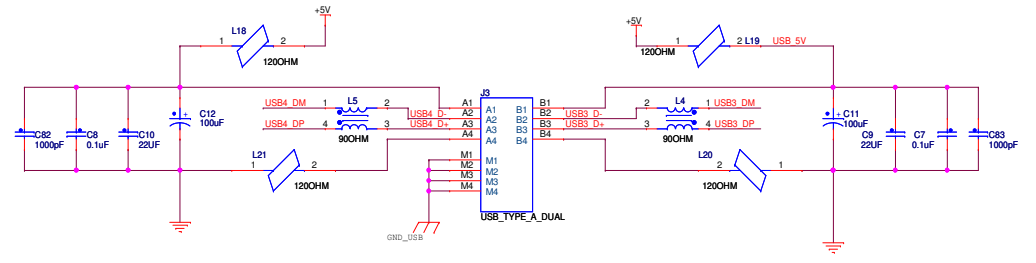
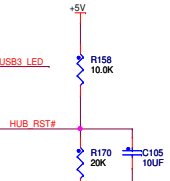
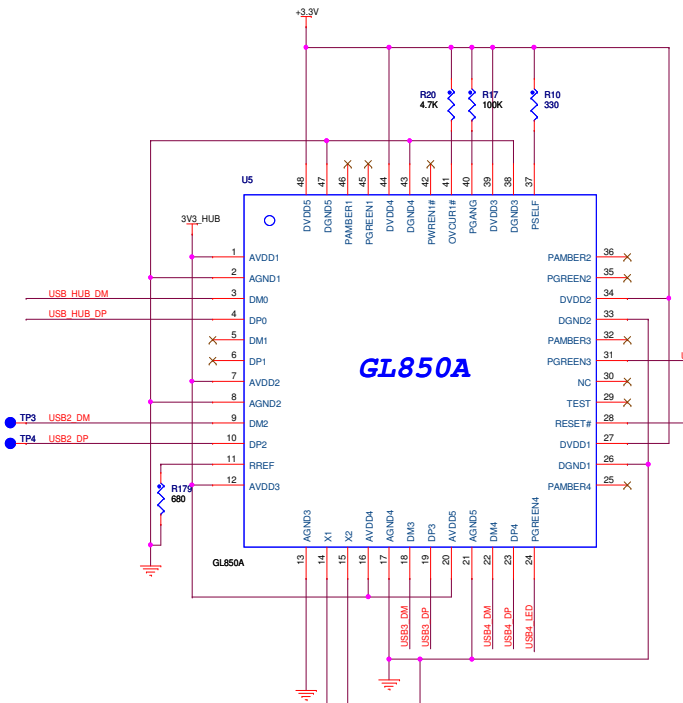
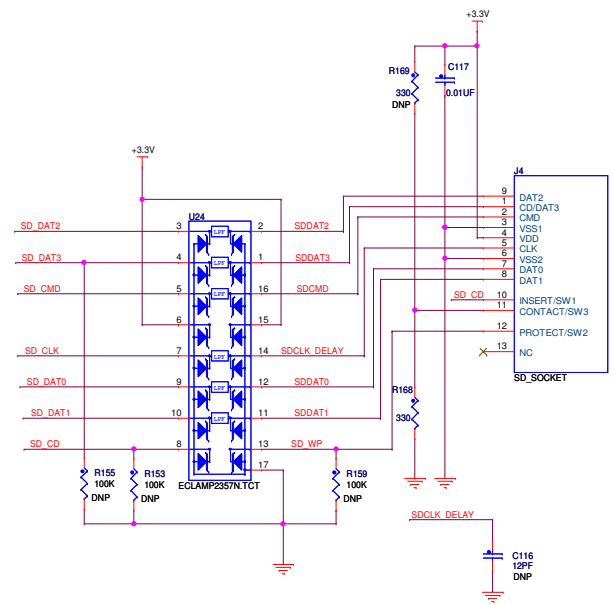
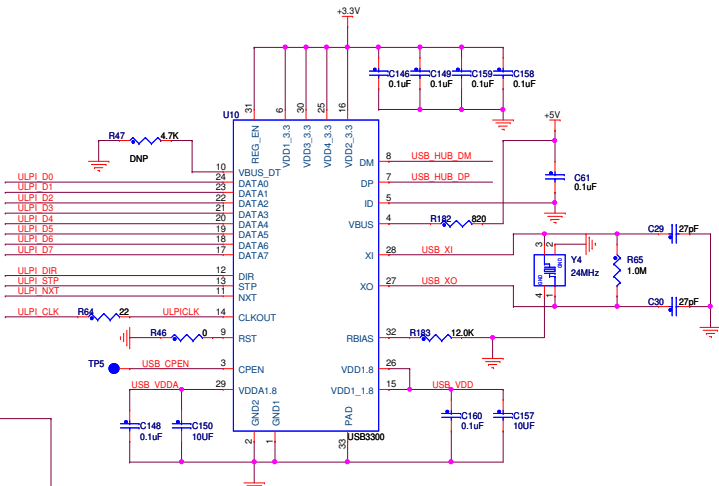
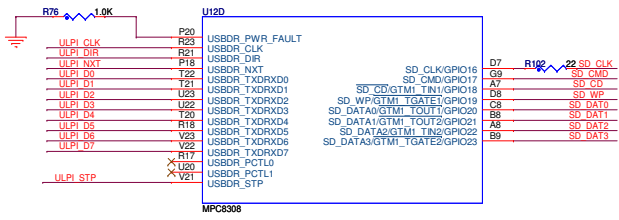
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Drawing Title:
MPC8308 - NSG

Page Title:
PCIE

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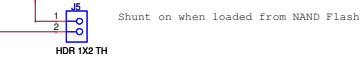
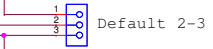
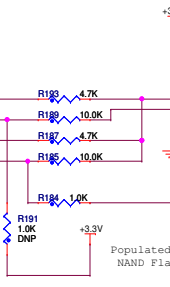
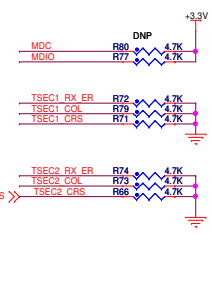
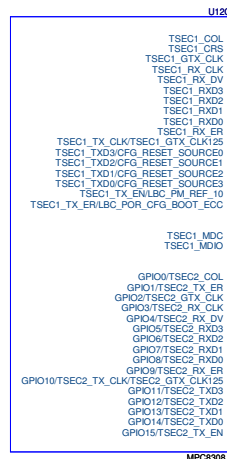


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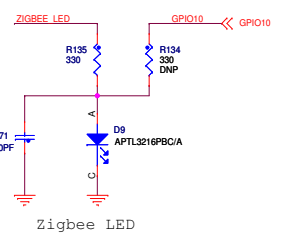
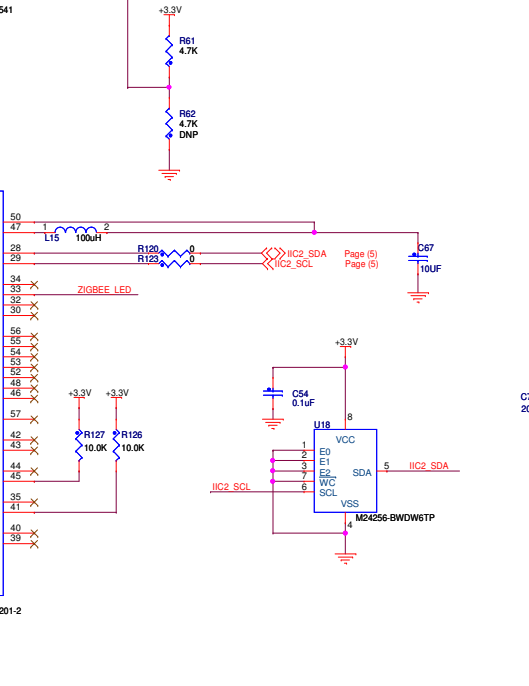
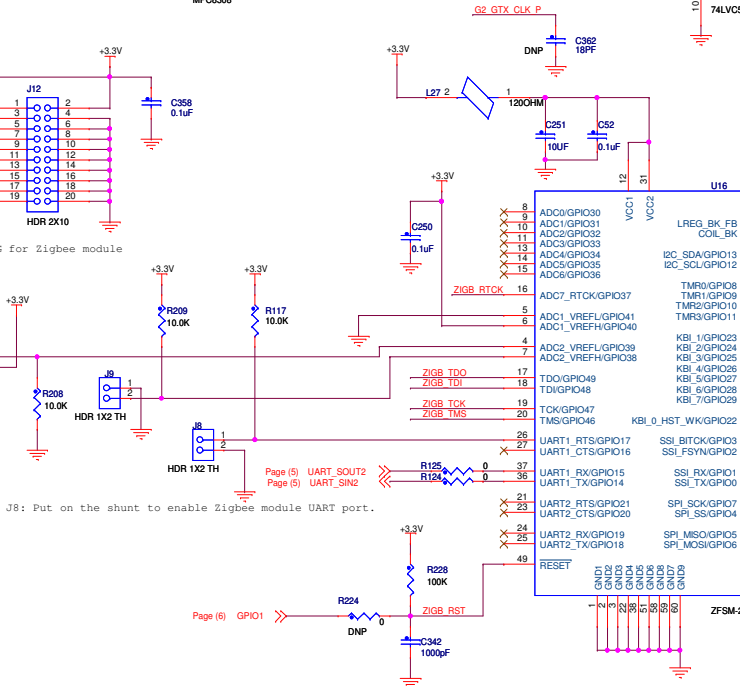
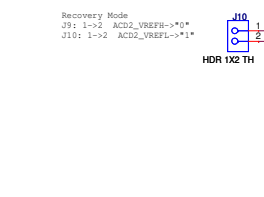
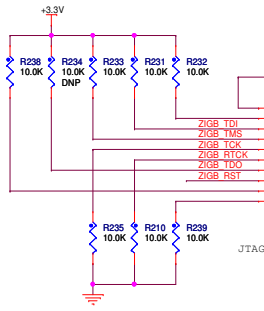
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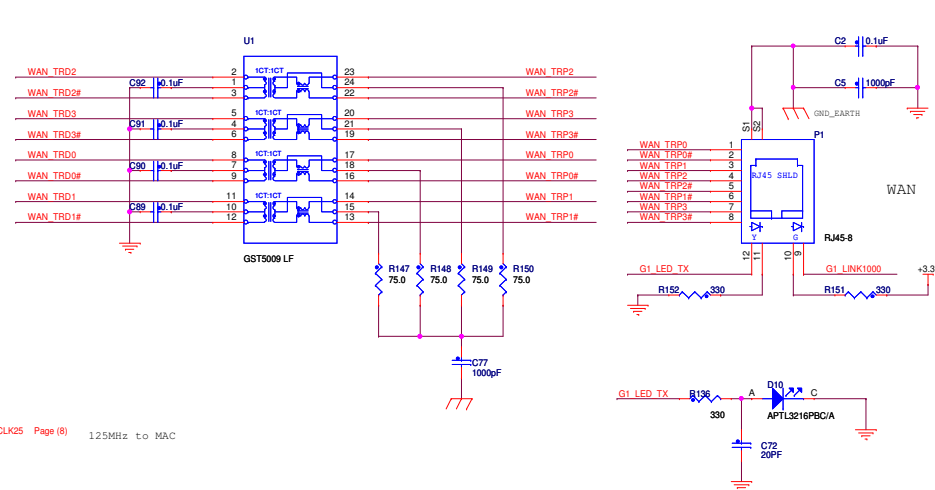
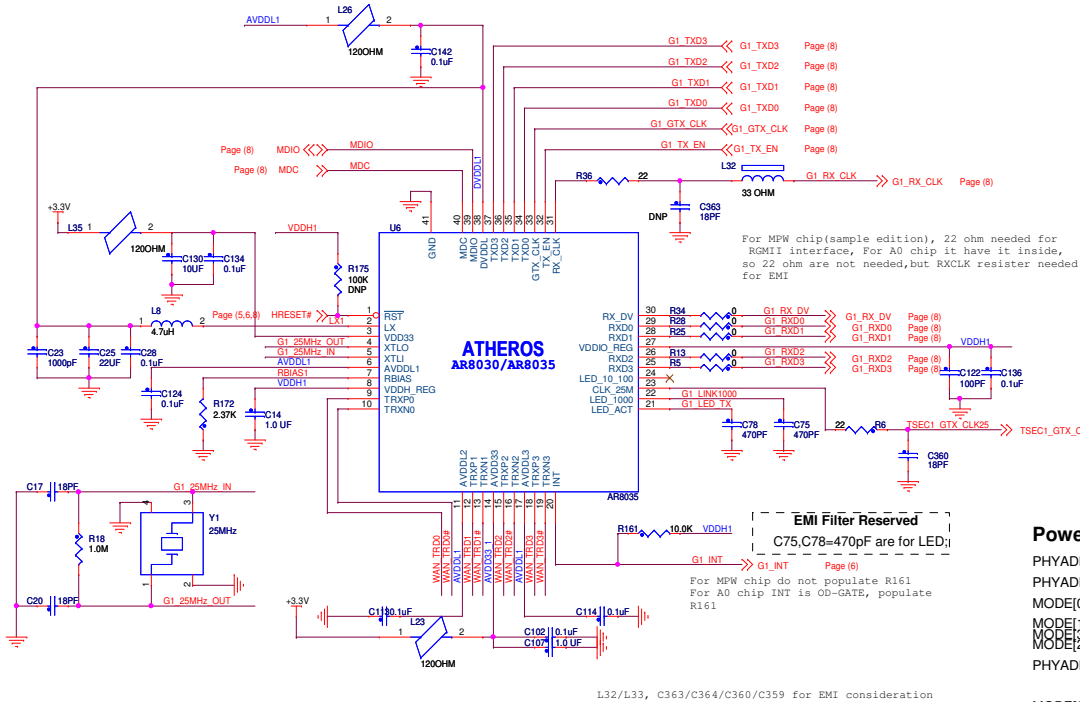
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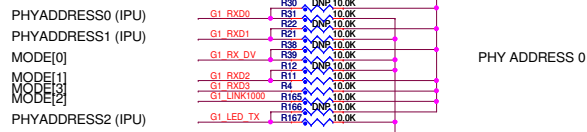
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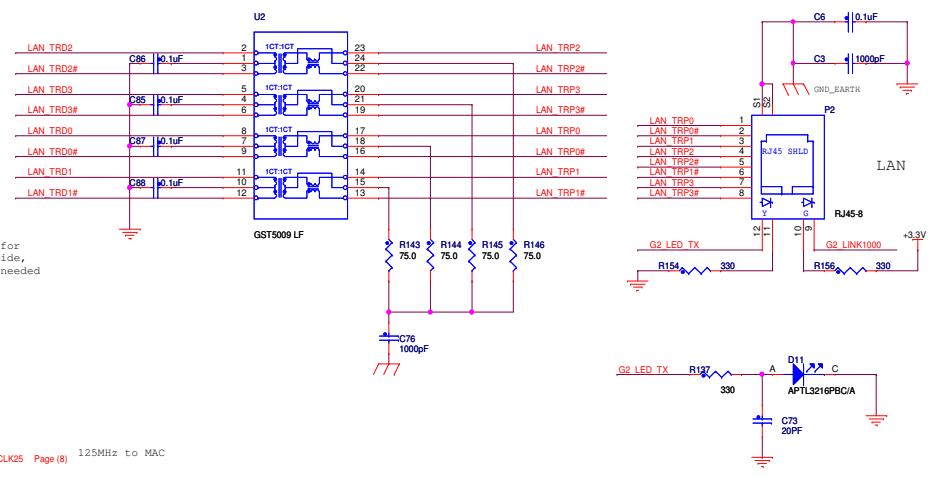
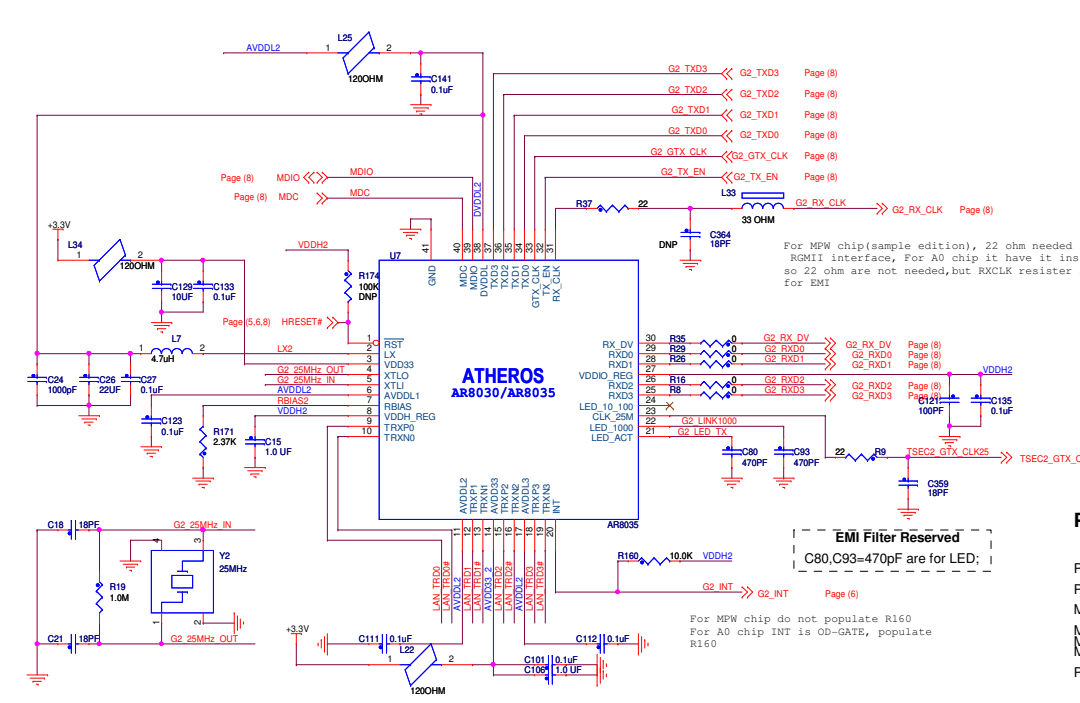
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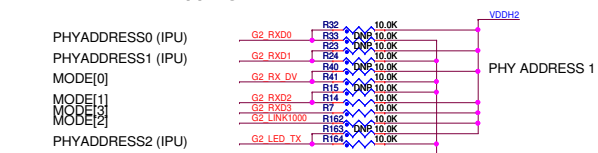
Power-on Strapping Pins



MODE[3:0]:
AR8035 default assemble:1110(RGMII)



Power-on Strapping Pins



MODE[3:0]:
AR8035 default assemble:1110(RGMII)

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ICAP Classification: FCP: FIUC: X PUBL:

Drawing Title:
MPC8308 - NSG

Page Title:
GBE PHY

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