S32K3安全和无线更新(OTA)

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2021年12月

SECURE CONNECTIONS
FOR A SMARTER WORLD

PUBLIC

AGENDA

- Introduction on OTA and Security
- Automotive Requirements
- Use Cases
- S32K Solution
- Summary

KEY DRIVERS FOR OVER THE AIR UPDATES

- Premium vehicles have over 100M lines of code! (Windows 10 has 50M)
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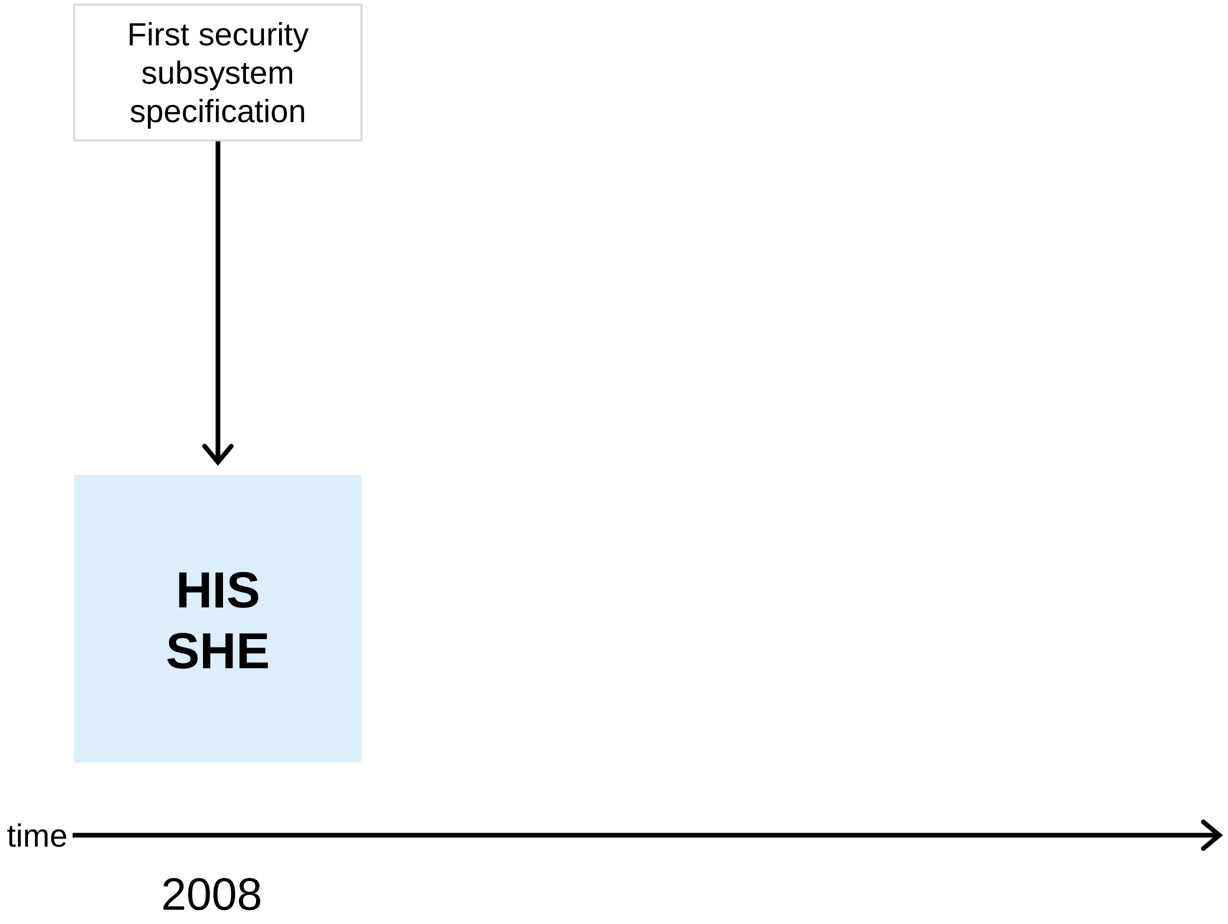
- Difficult to deliver new features to vehicle owners
- OEMs are missing post-purchase, revenue-generation opportunities

AUTOMOTIVE SECURITY SPECIFICATIONS

The SHE specification set the foundation, introducing the concept of a configurable (automotive) security subsystem



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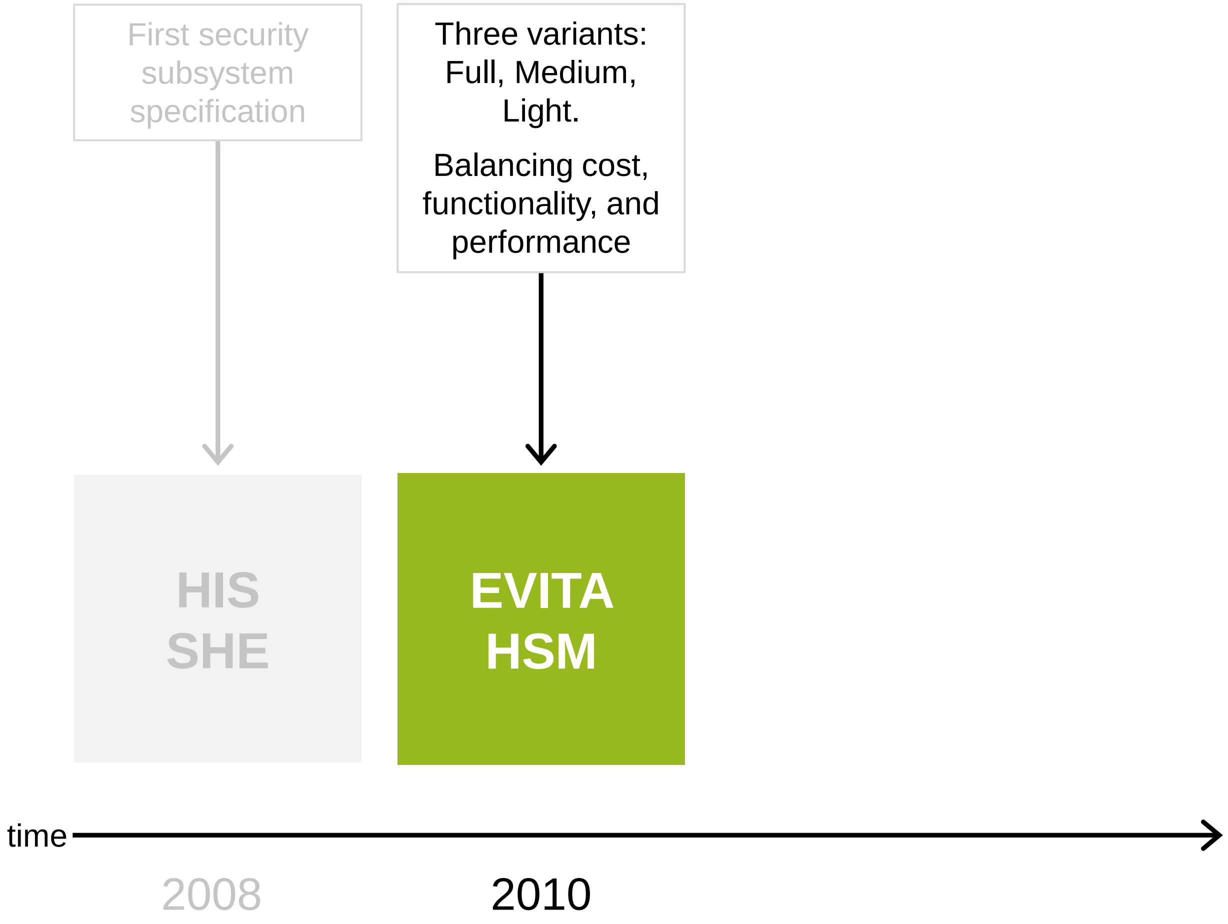

First security subsystem specification

Three variants: Full, Medium, Light.

Balancing cost, functionality, and performance

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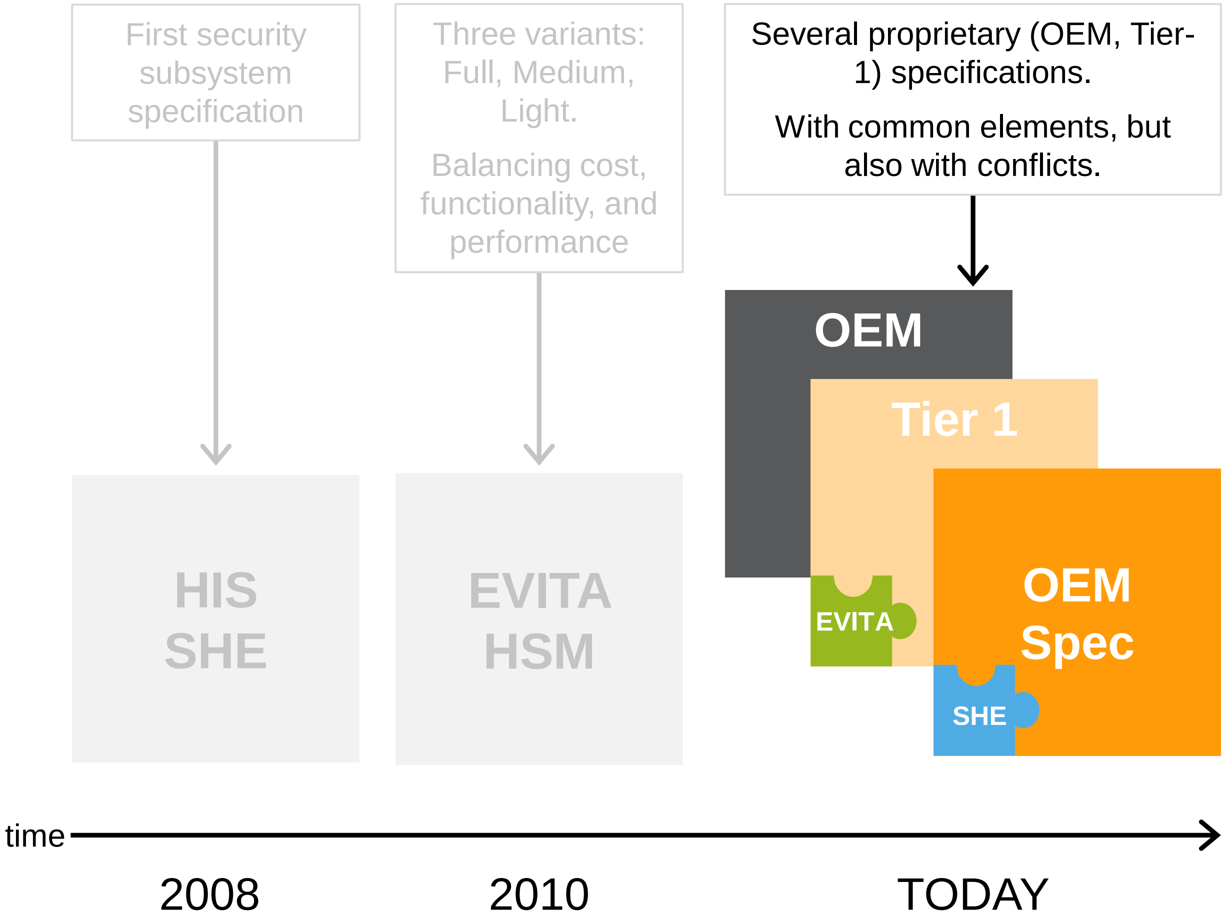
Nowadays, OEMs are creating their own technical specifications, including selected aspects of SHE, EVITA, and FIPS 140-2


First security subsystem specification
Three variants: Full, Medium, Light.
Balancing cost, functionality, and performance
Several proprietary (OEM, Tier-1) specifications.
With common elements, but also with conflicts.
HIS
SHE
EVITA
HSM
OEM
Tier 1
EVITA
OEM
Spec
SHE
time
2008
2010
TODAY

JULY 2021 UPDATE – UN R155 AND ISO 21434

From July 2022 onward, vehicle manufacturers must comply with the R155 automotive cybersecurity regulation for new vehicle type launches in Europe, Japan and Korea.

The standard **ISO/SAE 21434** is deemed very supportive in implementing the requirements on the Cyber Security Management System (CSMS), as specified in UN R155, in organizations along the supply chain.

NXP therefore aims at supporting the OEMs, as well as its direct (Tier-1) customers, by ensuring organizational compliance with the standard and by ensuring that new (future) products are developed in compliance with the standard. Additionally, existing products will be supported by the associated processes of our CSMS (PSIRT etc.).

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- **To keep up against malicious attacks, Security must remain up to date**

  → Security sub system must be updatable

OTA and Security Use Cases in Automotive

OVER THE AIR (OTA) UPDATE METHODS

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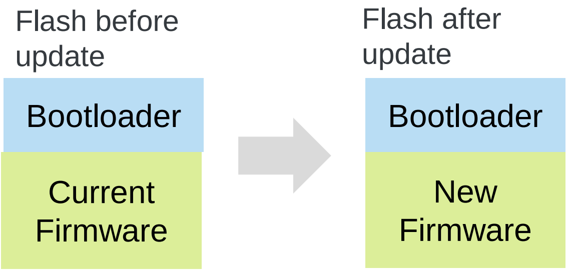

Flash before update

Bootloader

Current Firmware

Flash after update

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New Firmware

A/B

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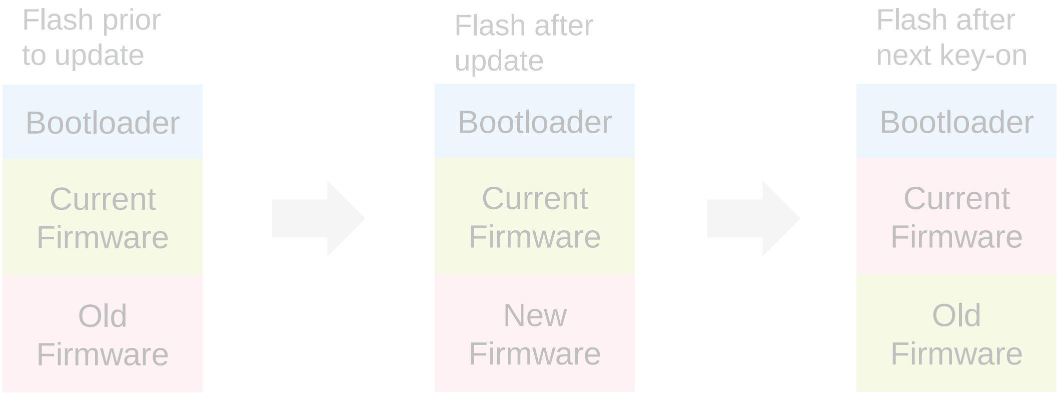

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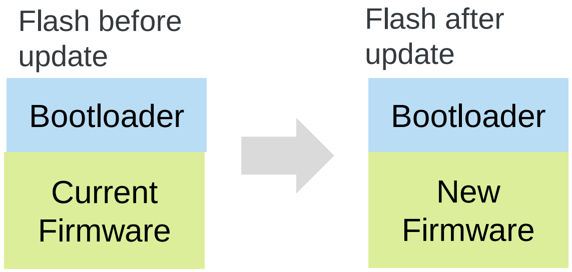

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- No need for additional flash

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- Requires vehicle downtime during update process
- Not possible to instantly “roll-back” if an issue occurs
- Higher risk to have an ECU inoperable

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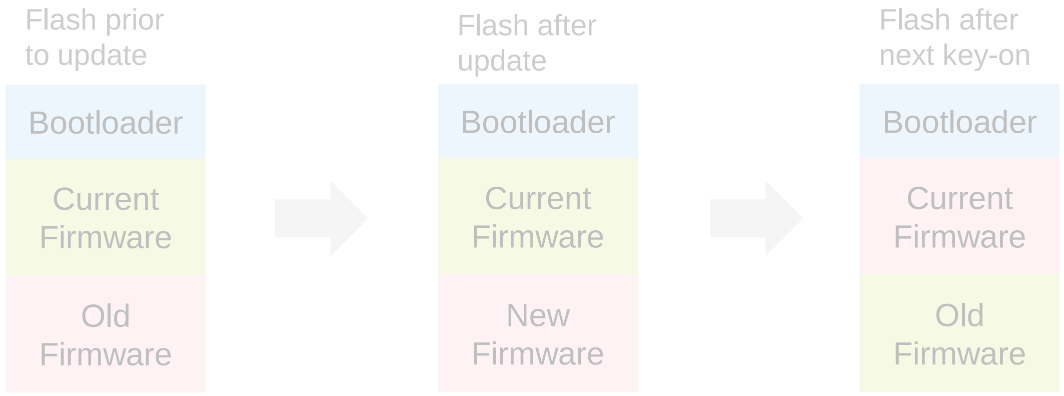

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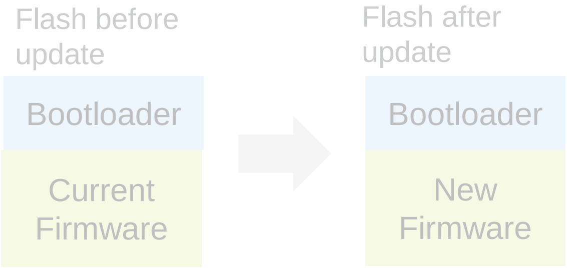

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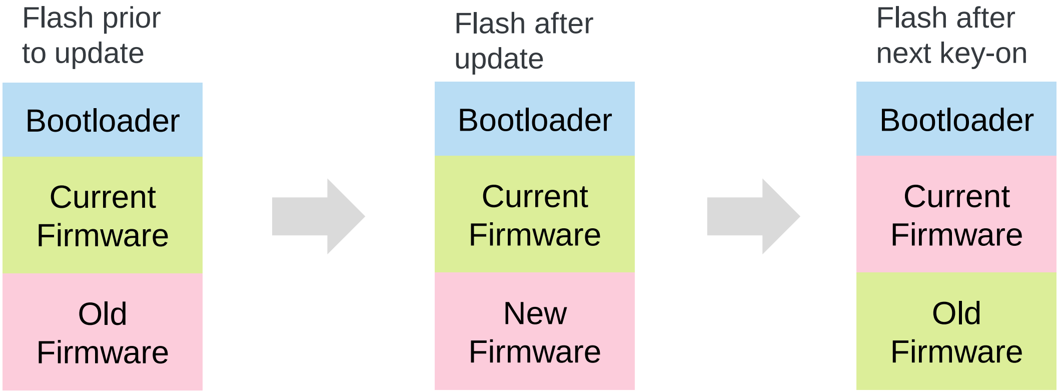

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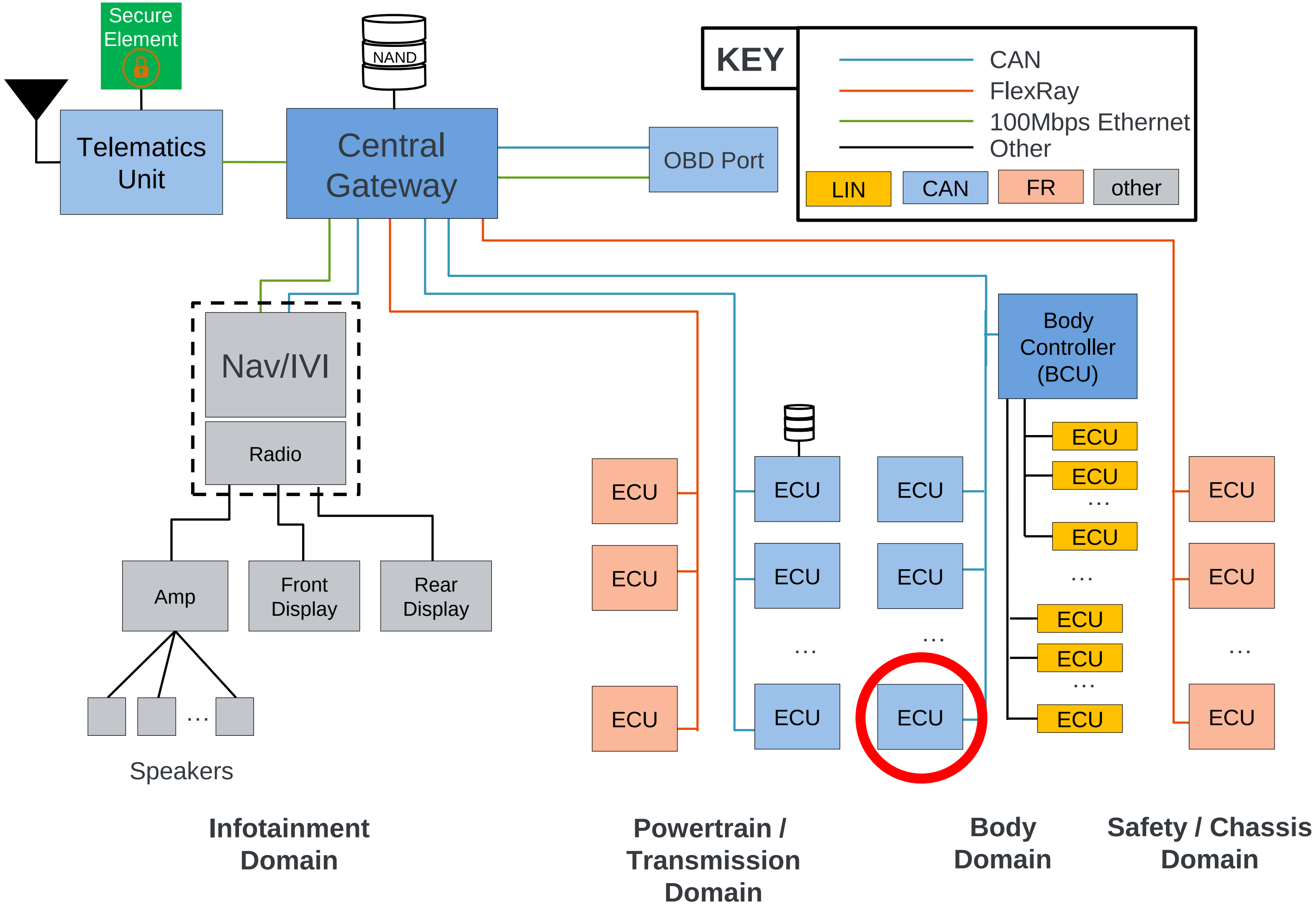
Advantages

- Update can be carried out whilst application is actively running from flash
- Always have original firmware to roll back to in case of issue
- Vehicle always available – guaranteed no vehicle downtime regardless of update errors

Cost

- Requires 2x flash application storage
- Higher max current (run current in block A + erase/program current in block B)

OTA USE CASE: 2 FW VERSIONS IN INTERNAL MEMORY



Example ECU A

Flash: 2x internal flash available

Security: Supports CMAC authentication and AES-128 decryption

Connection to Gateway: Ethernet

Vehicle Downtime: **none**

Security: **high**

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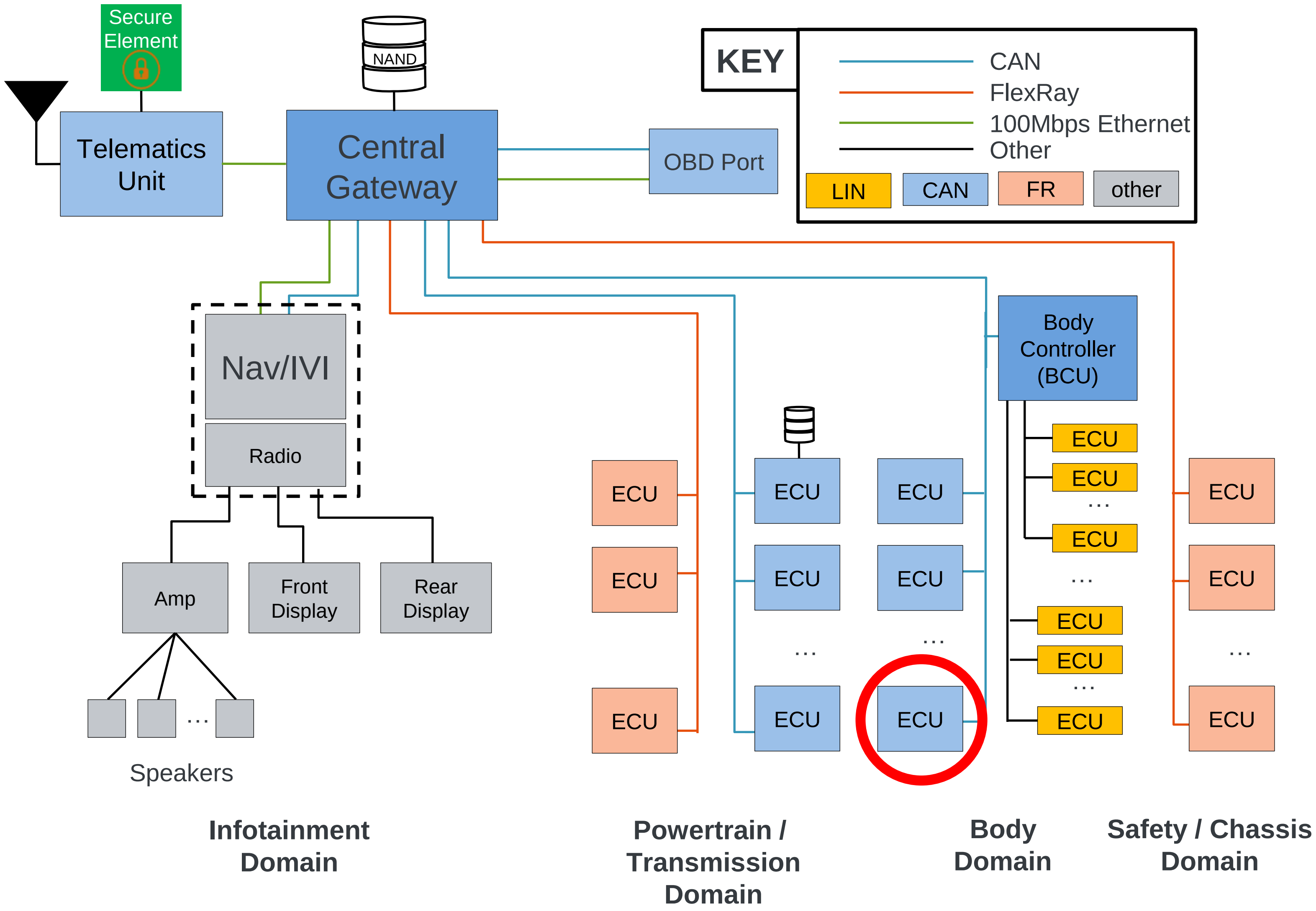

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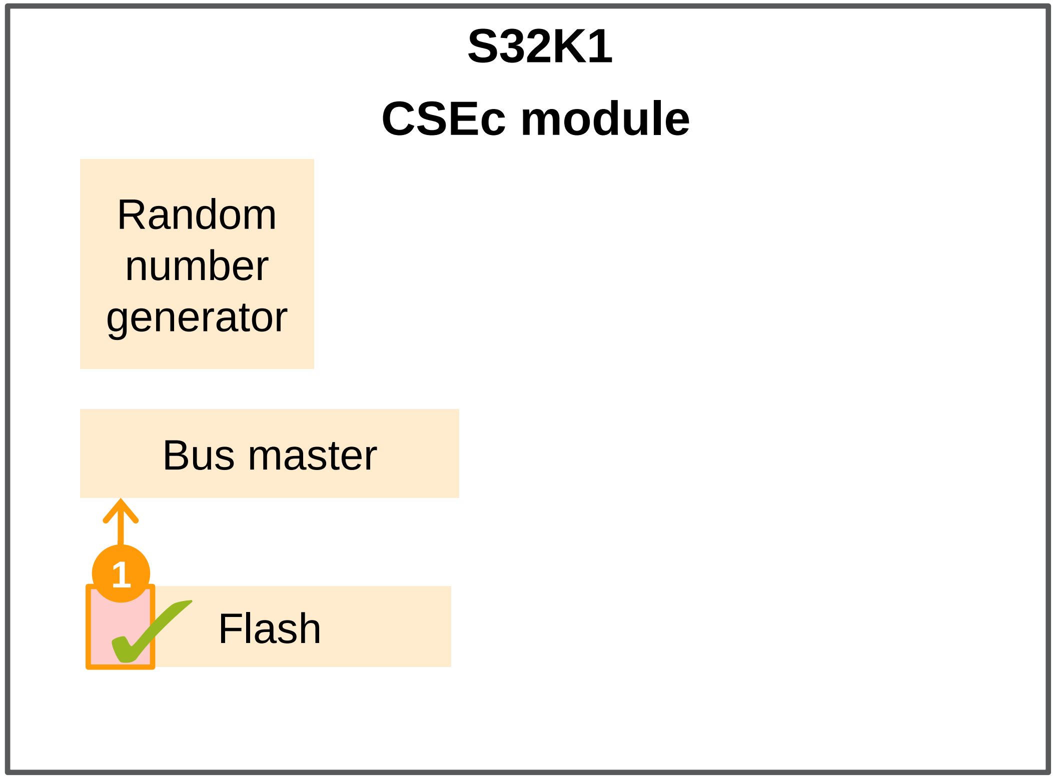
Steps:

- Encrypted binary trickle downloaded and stored onto empty “B” flash on ECU.
- Firmware is decrypted and integrity checked as it is downloaded. Allows end-to-end security
- Once download complete, GW switches ECU to use new firmware from next boot

SECURE BOOT - CHECK BOOT LOADER FOR INTEGRITY AND AUTHENTICITY ON S32K1

Step 1: After power on: CSE module reads bootloader via its bus master interface.



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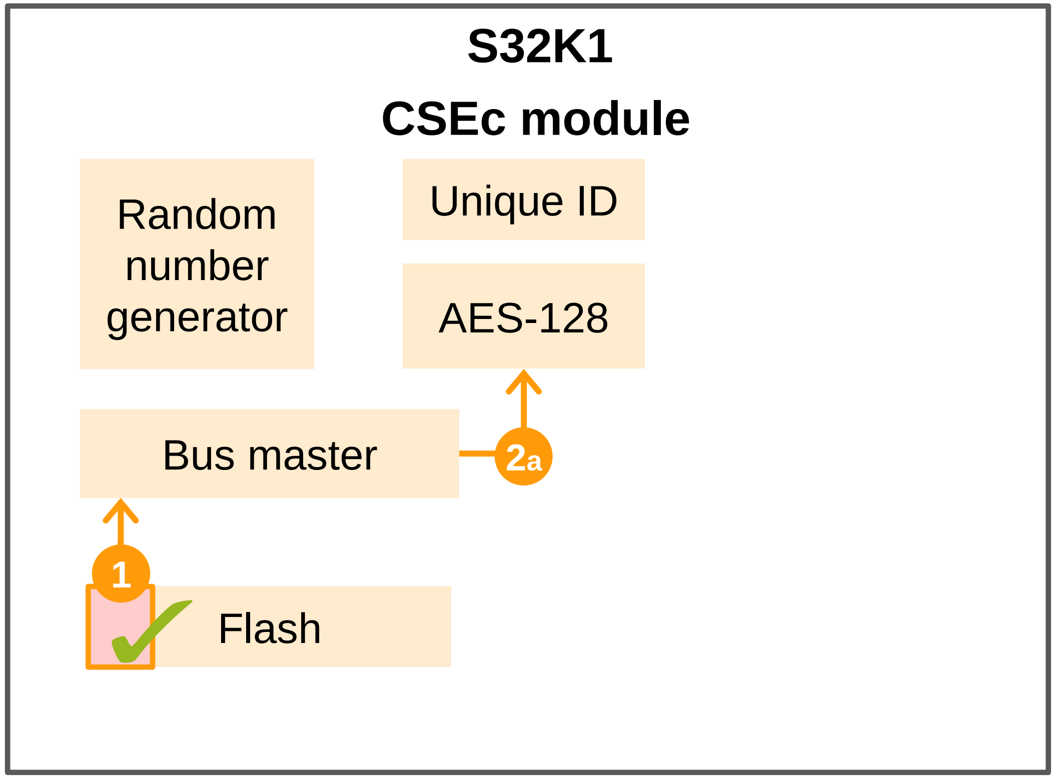

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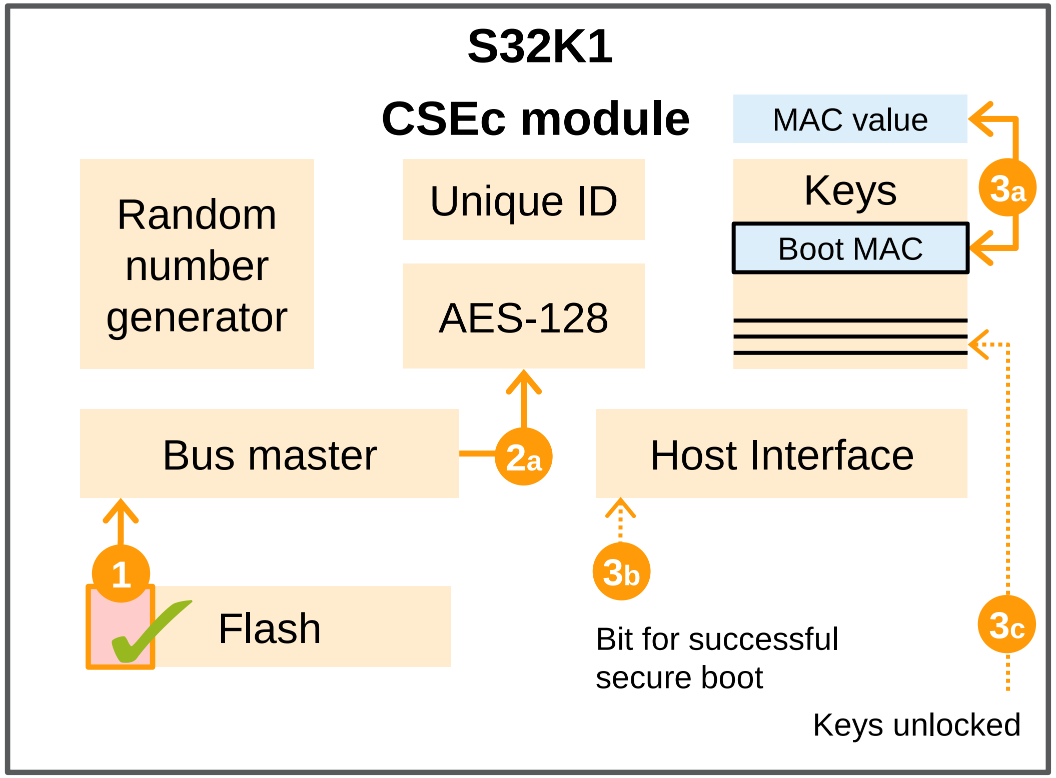

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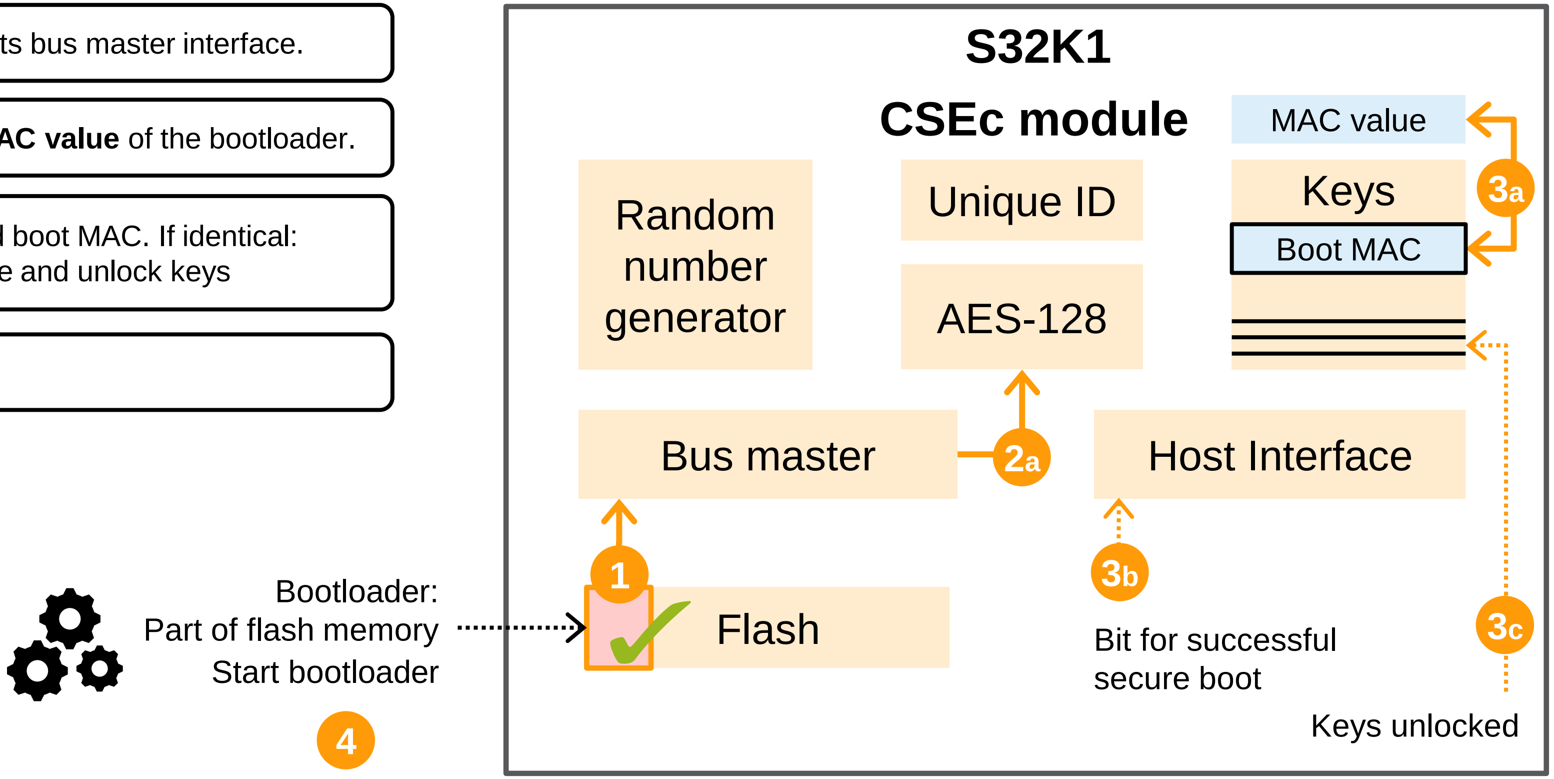

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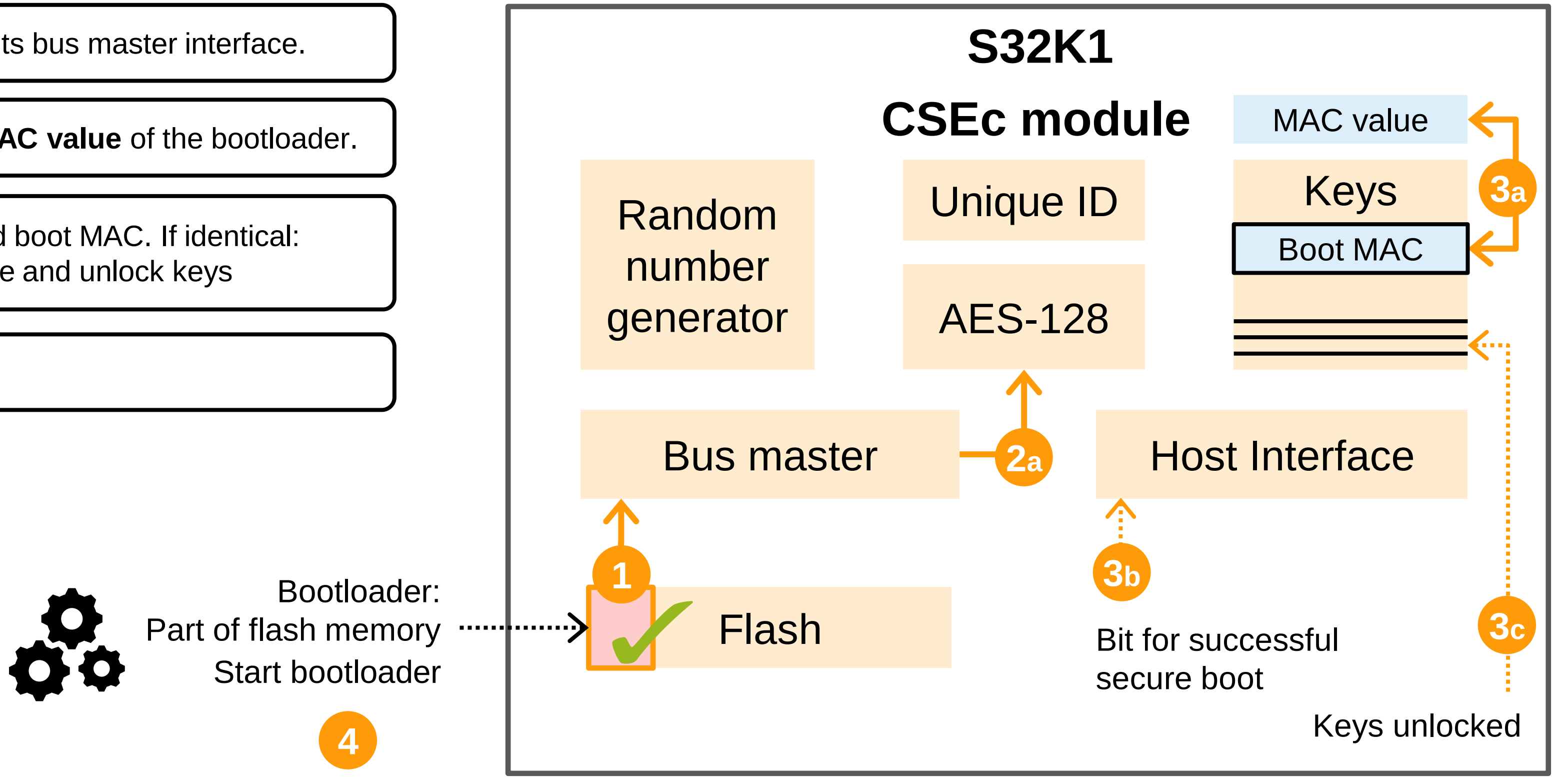
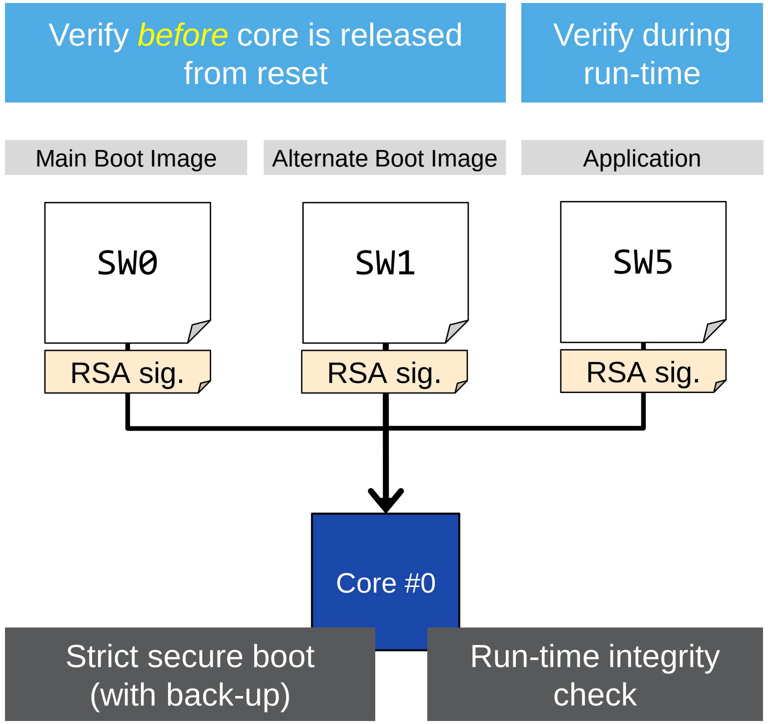


- **MAC** protects against modification of bootloader and depends on the (secret) boot key → integrity and authenticity of bootloader.
- Only if calculated MAC value matches stored boot MAC value: successful secure boot → set respective bit in host interface and unlock keys for further usage (see next demos)

SECURE BOOT CONFIGURATION EXAMPLE WITH S32K3



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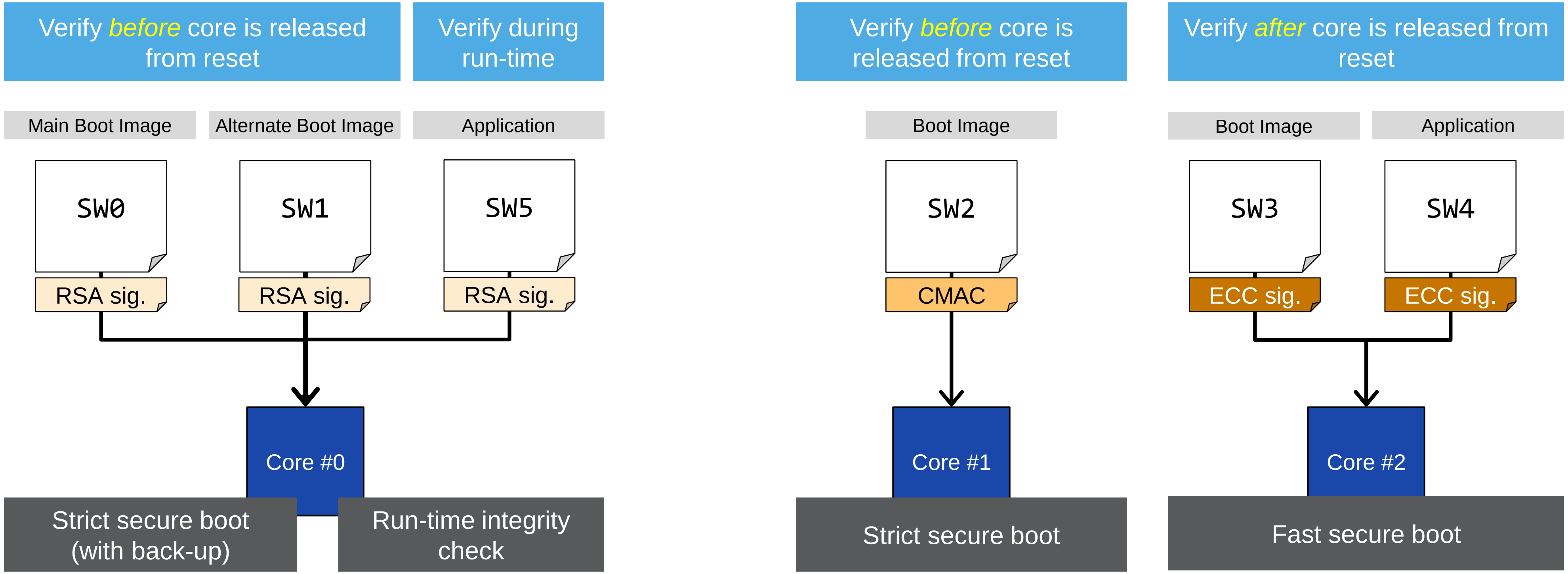

Verify *before* core is released from reset

Verify during run-time

Main Boot Image

Alternate Boot Image

Application

SW0

SW1

SW5

RSA sig.

RSA sig.

RSA sig.

Core #0

Strict secure boot (with back-up)

Run-time integrity check

Verify *before* core is released from reset

Boot Image

SW2

CMAC

Core #1

Strict secure boot

Verify *after* core is released from reset

Boot Image

Application

SW3

SW4

ECC sig.

ECC sig.

Core #2

Fast secure boot

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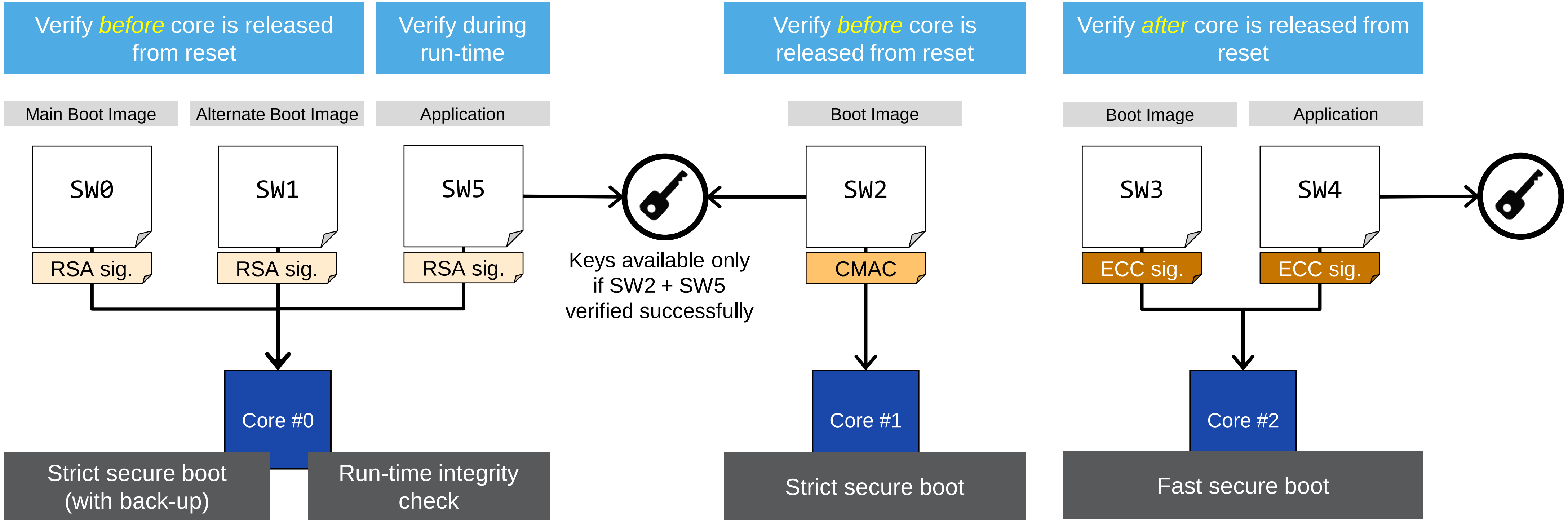

→ Allows Versatile Verification Methods, Multiple Startup Orders and Sanctions ←

OTA and Security Automotive Requirements

OVER THE AIR UPDATES REQUIREMENTS

ECU reprogramming outside garage.
Seamless update for driver (zero down time).

Seamless update

- Download while application running
- Zero down time
- Zero installation time

Memory features

- Read while write between flash banks.
- Automatic firmware address translation.
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- Multiple version of firmware available.

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Opens a door for security vulnerability.

Attack protection

- Against firmware stealing.
- Against malicious firmware installation.

Security hardware

- Encryption/ decryption of data.
- Firmware authentication check.

SECURITY REQUIREMENTS – TODAY'S LANDSCAPE

	SHE	EVITA (Light / Medium / Full)	More recent needs
ARCHITECTURE	• Configurable, fixed function	• Programmable (except EVITA Light)	• Acceleration close to the interfaces (CAN and ETH MAC/PHYs) • Support for Flash-less technologies
FUNCTIONALITY	• Secure boot • Memory update protocol • AES-128 (ECB, CBC) • CMAC, AES-MP • TRNG, PRNG • Key derivation (fixed algorithm) • 10+4 keys, key-usage flags	Same as SHE, plus: • AES-PRNG • monotonic counters (16x, 64bit) Plus, for EVITA Medium and Full: • WHIRLPOOL, HMAC-SHA1, ECDH and ECDSA (P256)	• Further crypto algorithms (e.g. RSA, SHA1-3, Curve25519, …) • Rollback protection • Key negotiation protocols • Communication protocol offloading (e.g. TLS, IPsec, MACsec, …) • Context separation / multi-application scenarios
OTHER			• Increased attack resistance (e.g. SCA, Fault Injection, …)
Covered by:	NXP CSE family (since 2010)		
	NXP HSM family (since 2015)		
	NXP HSE family (since 2019)		

S32K Solution

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S32K offers the most complete OTA portfolio

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- In place support

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- Secure firmware version control in hw
- Brownout and communication monitor in hw by **Firmware indicator validation**

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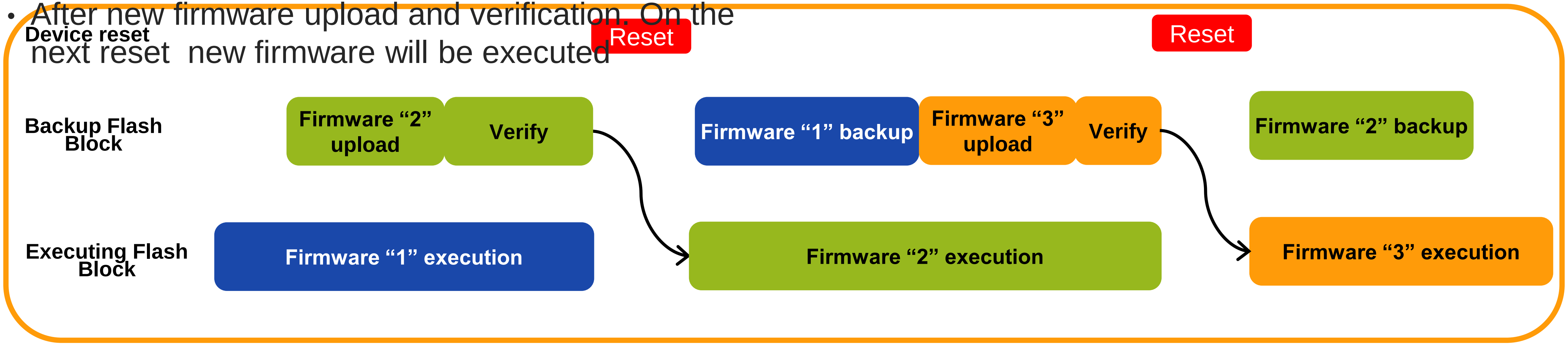
Use case: A/B swap in internal flash

- Current firmware executes and simultaneously uploads new firmware image into backup flash block
- After new firmware upload and verification. On the next reset new firmware will be executed

S32K3xx Firmware Update



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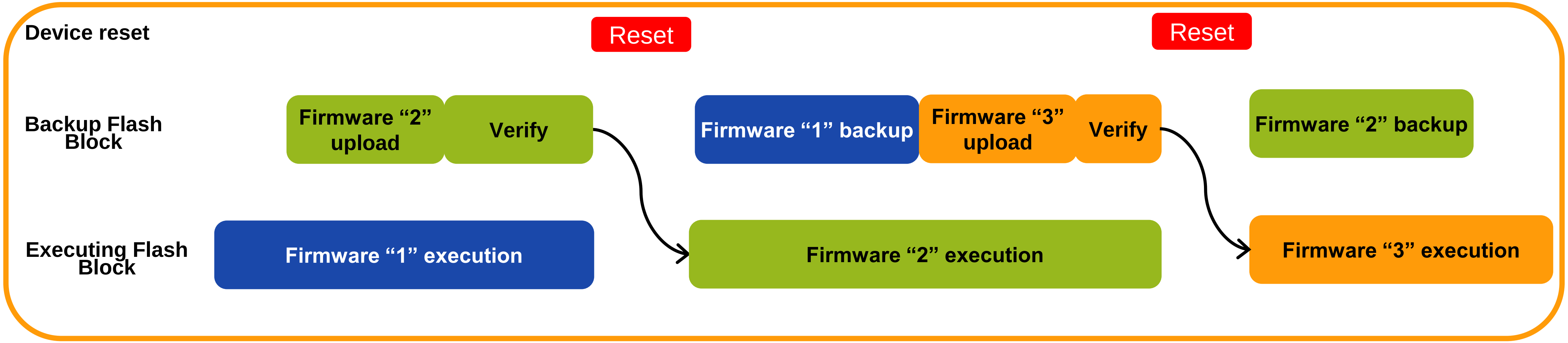
S32K3 Value

- Zero downtime, instant A/B swap after reset
- Download while application running
- Automatic address translation
- Backup firmware available

S32K3xx Firmware Update



S32K1 AND S32K3 FEATURE SET

S32K1

Basic set of cryptographic functions for SHE support

20 keys
SHE update key protocol

SHE memory authenticity checks during start-up (CMAC)

S32K1 AND S32K3 FEATURE SET

S32K1	Basic set of cryptographic functions for SHE support	20 keys SHE update key protocol	SHE memory authenticity checks during start-up (CMAC)	
S32K3	Comprehensive cipher suite SHA-2, SHA-3, RSA and ECC support	Configurable set of keys Extensive key management (import, export, derive)	Extended memory authenticity checks during boot & run-time	Monotonic counters Secure tick

SECURITY LEADERSHIP – PROVEN EXTENSIVE SECURITY EXPERIENCE

Proven Extensive Security Experience

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- High security industry:
  - Leadership in banking card, e-passport, mobile payment

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- Auto:
  - First to implement SHE security on silicon (2010)
  - All MPU/MCUs 2017 onward include crypto hardware
  - **ISO 21434**: NXP cybersecurity engineering processes are now certified as compliant with the new automotive cybersecurity standard ISO/SAE 21434. (Certified by TÜV SÜD)

Root of Trust & Trusted Process

SECURITY LEADERSHIP – ROOT OF TRUST & TRUSTED PROCESS

Root of Trust & Trusted Process

- Secure Trust Provisioning in non-secure production environment

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Root of Trust & Trusted Process

- Secure Trust Provisioning in non-secure production environment
- BootROM used to establish the Root of Trust during manufacturing

SECURITY LEADERSHIP – PRODUCT SECURITY INCIDENT RESPONSE TEAM

Product Security Incident Response Team

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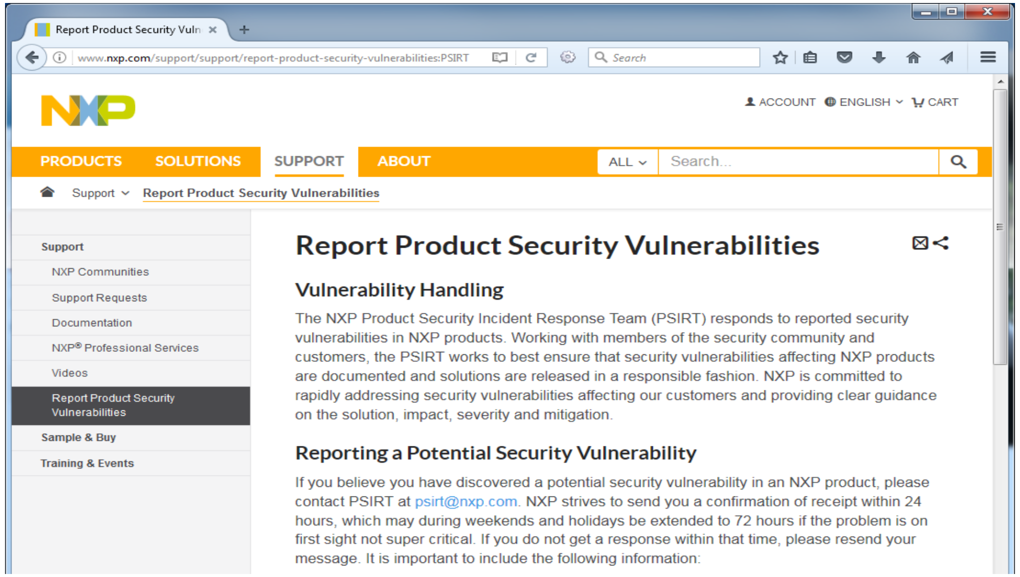
Report Product Security Vuln
www.nxp.com/support/support/report-product-security-vulnerabilities:PSIRT
Search
ACCOUNT
ENGLISH
CART
PRODUCTS
SOLUTIONS
SUPPORT
ABOUT
ALL
Search...
Support
Report Product Security Vulnerabilities
Support
NXP Communities
Support Requests
Documentation
NXP® Professional Services
Videos
Report Product Security Vulnerabilities
Sample & Buy
Training & Events

Report Product Security Vulnerabilities

Vulnerability Handling

The NXP Product Security Incident Response Team (PSIRT) responds to reported security vulnerabilities in NXP products. Working with members of the security community and customers, the PSIRT works to best ensure that security vulnerabilities affecting NXP products are documented and solutions are released in a responsible fashion. NXP is committed to rapidly addressing security vulnerabilities affecting our customers and providing clear guidance on the solution, impact, severity and mitigation.

Reporting a Potential Security Vulnerability

If you believe you have discovered a potential security vulnerability in an NXP product, please contact PSIRT at psirt@nxp.com. NXP strives to send you a confirmation of receipt within 24 hours, which may during weekends and holidays be extended to 72 hours if the problem is on first sight not super critical. If you do not get a response within that time, please resend your message. It is important to include the following information:

Contact: www.nxp.com/psirt, psirt@nxp.com

Product Security Incident Response Team

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- Confirmation of receipt within 24 hours
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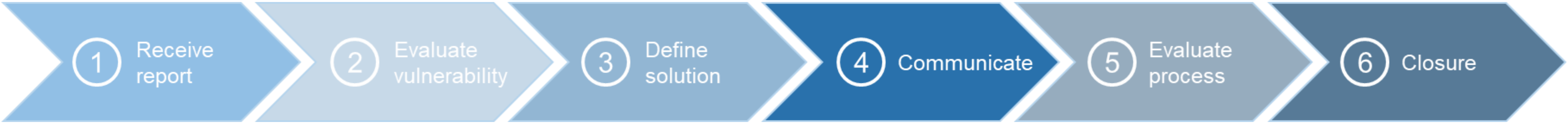

Incident response process

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- Committed to Responsible Disclosure
- Security intelligence sharing with Auto ISAC

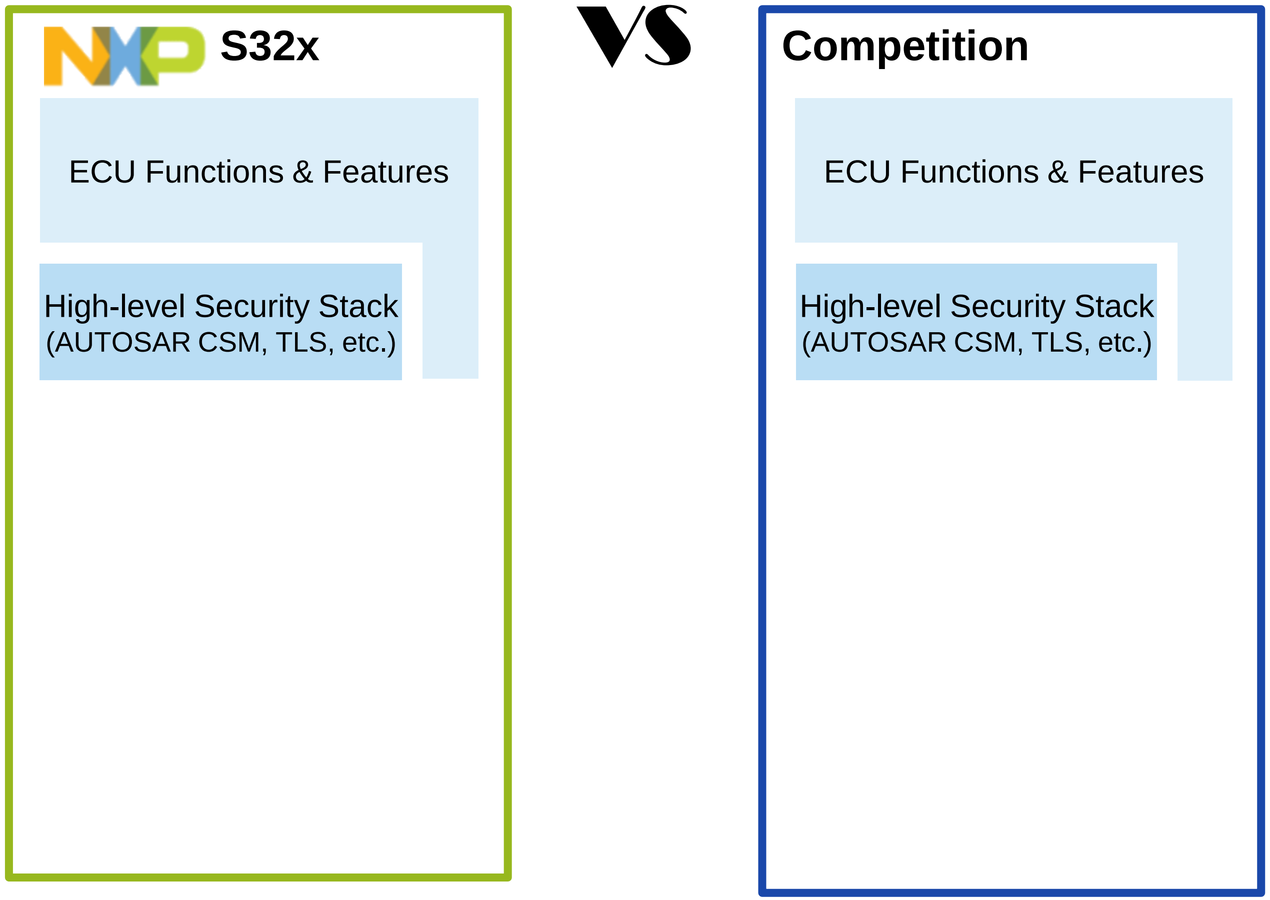
S32K3 SECURITY OFFER IS SIMPLER

Comprehensive service offer

- FAE support
- FQE analysis
- PSIRT
- Standard crypto-driver: MCAL AUTOSAR

One-stop-shop (HW + FW)
Cost-optimized solution

Two suppliers (HW / FW)
Higher solution cost & complexity


NXP S32x
ECU Functions & Features
High-level Security Stack (AUTOSAR CSM, TLS, etc.)
VS
Competition
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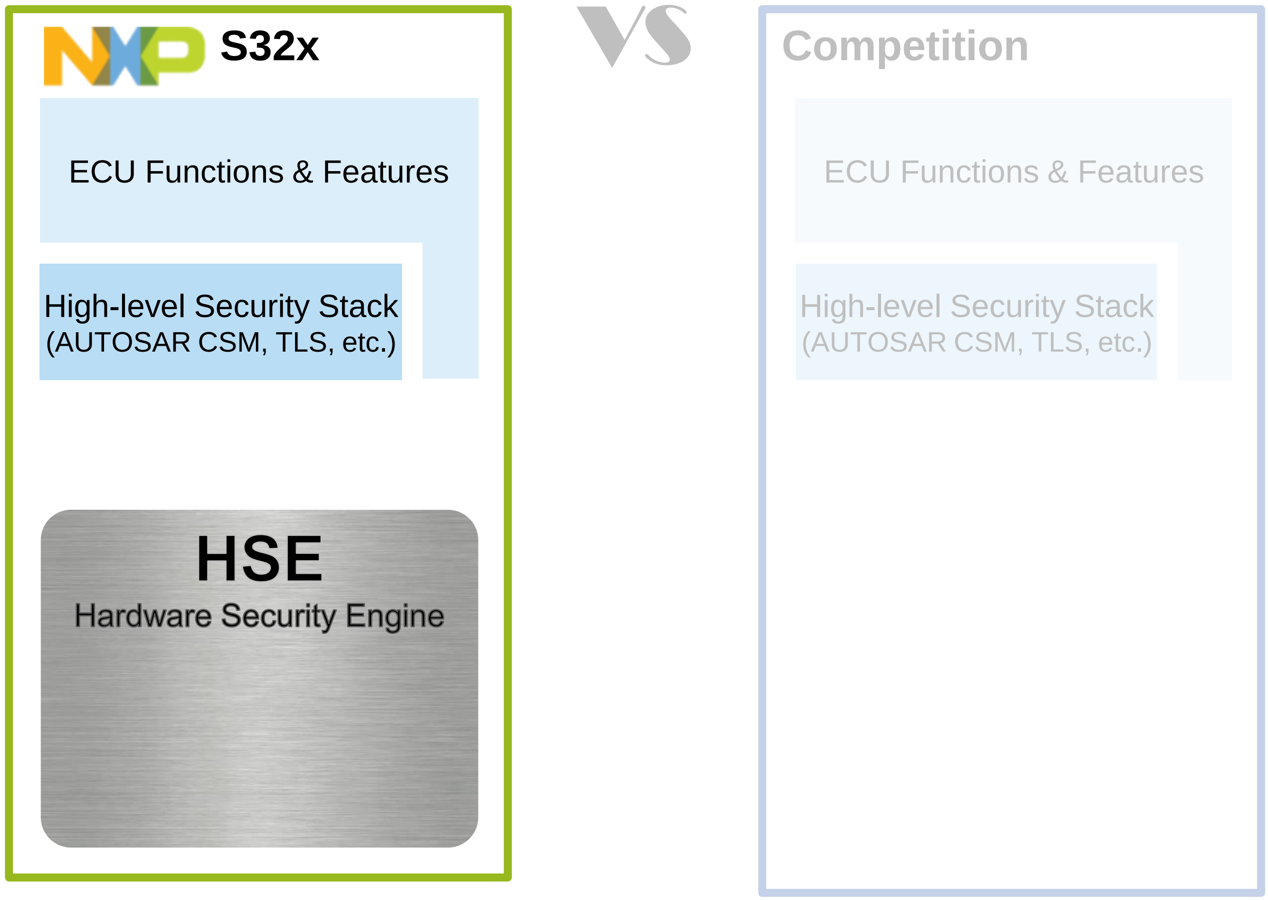

S32x

ECU Functions & Features

High-level Security Stack
(AUTOSAR CSM, TLS, etc.)

HSE
Hardware Security Engine

VS

Competition

ECU Functions & Features

High-level Security Stack
(AUTOSAR CSM, TLS, etc.)

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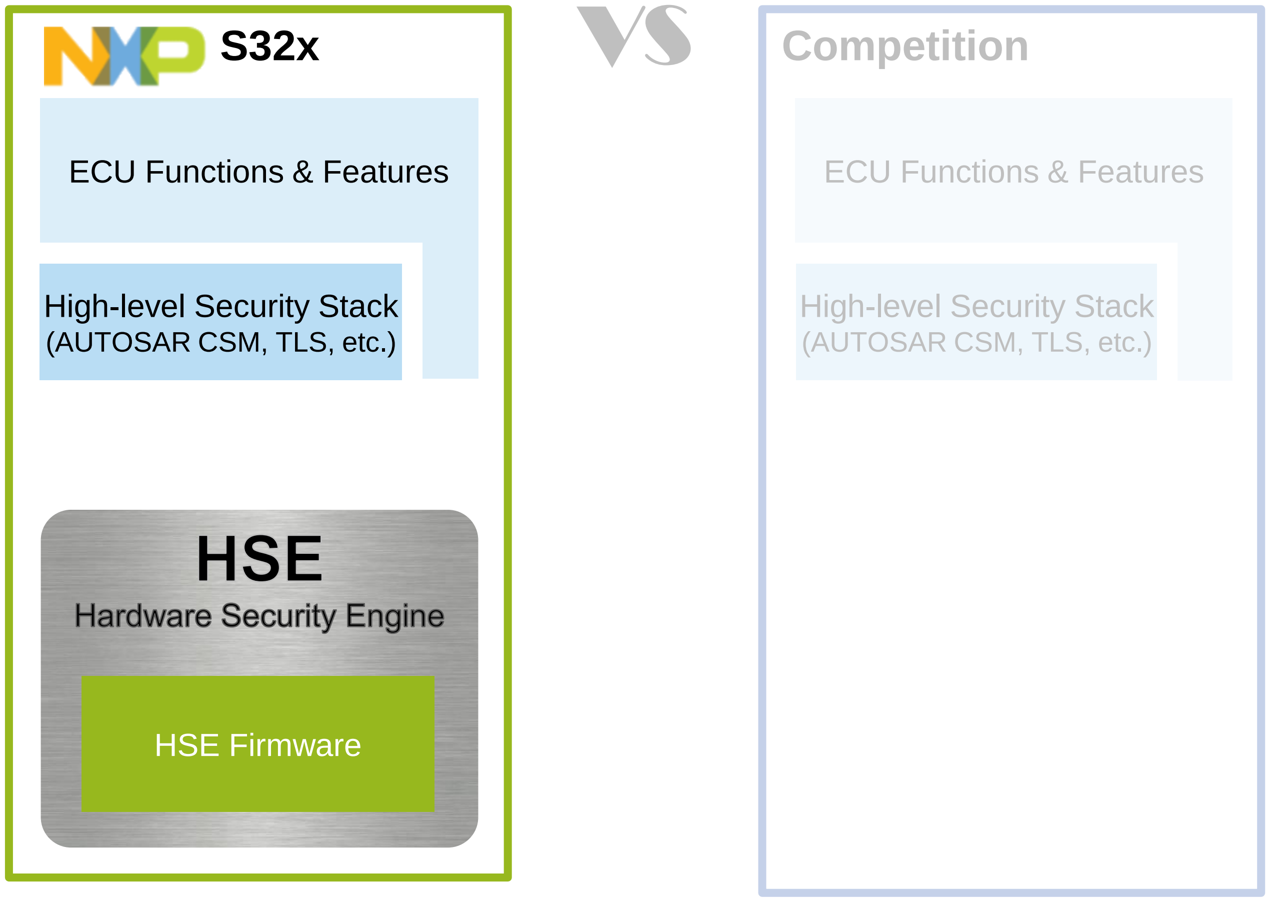

S32K3 SECURITY OFFER IS SIMPLER

Comprehensive service offer

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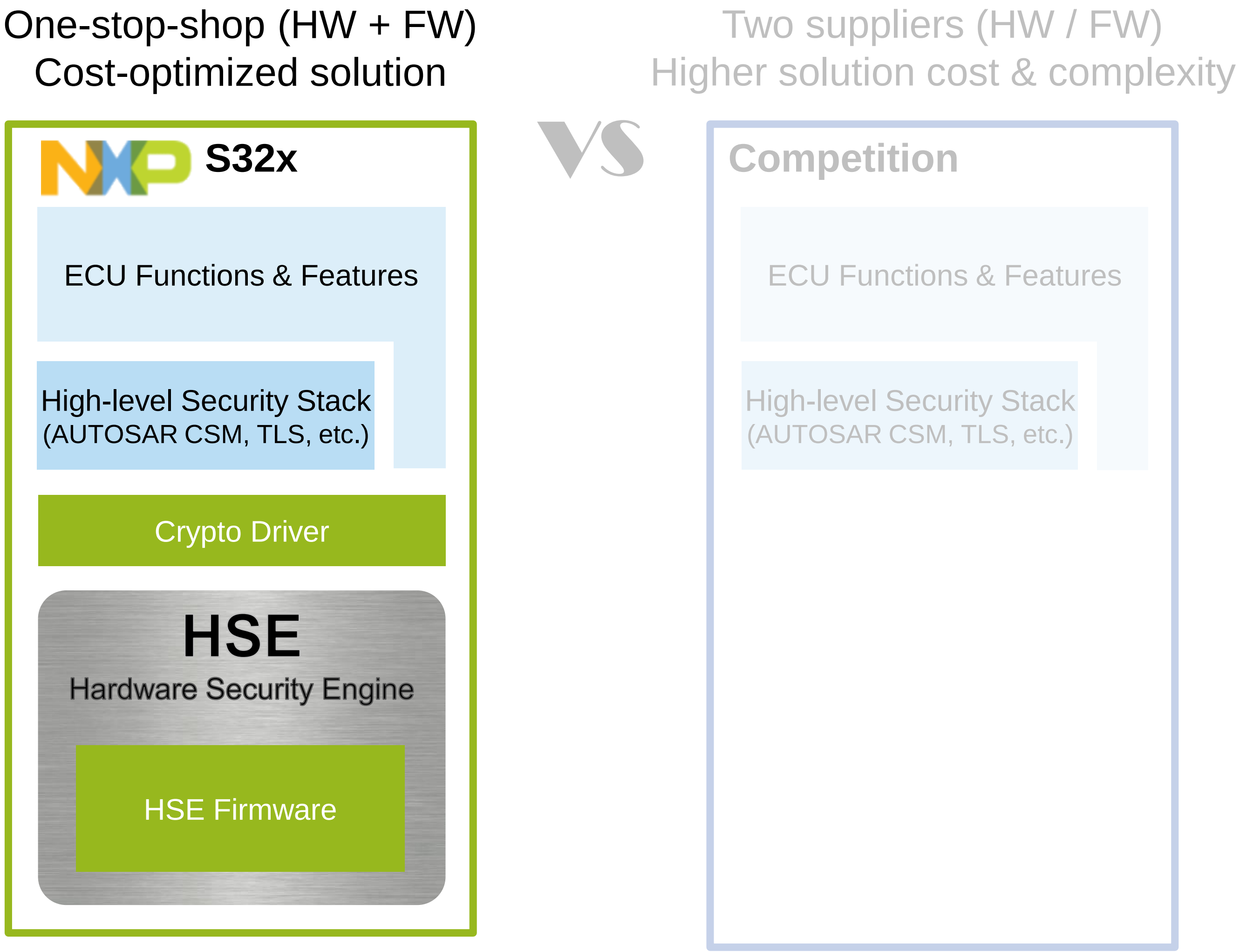
- FQE analysis
- PSIRT
- Standard crypto-driver: MCAL AUTOSAR



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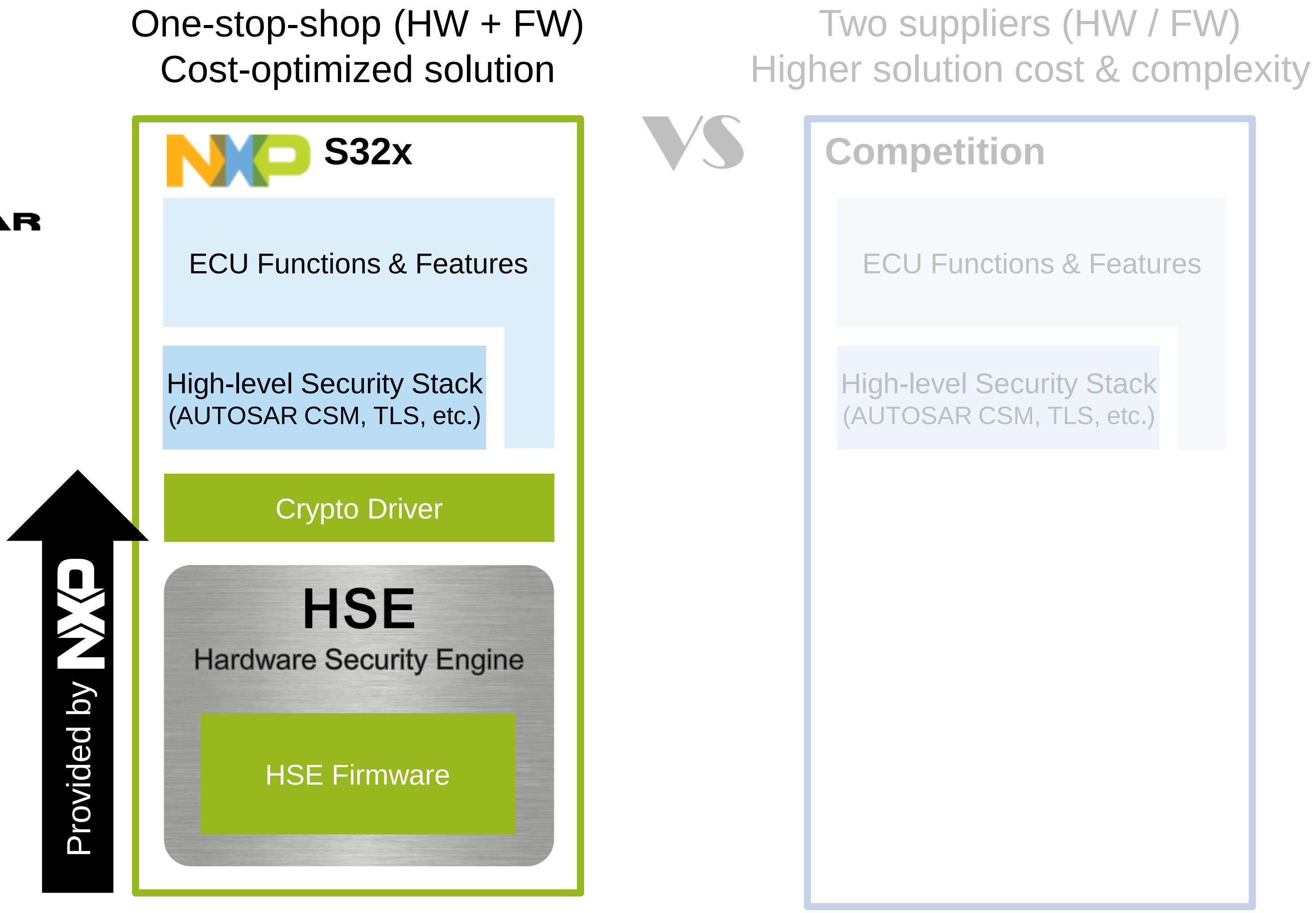

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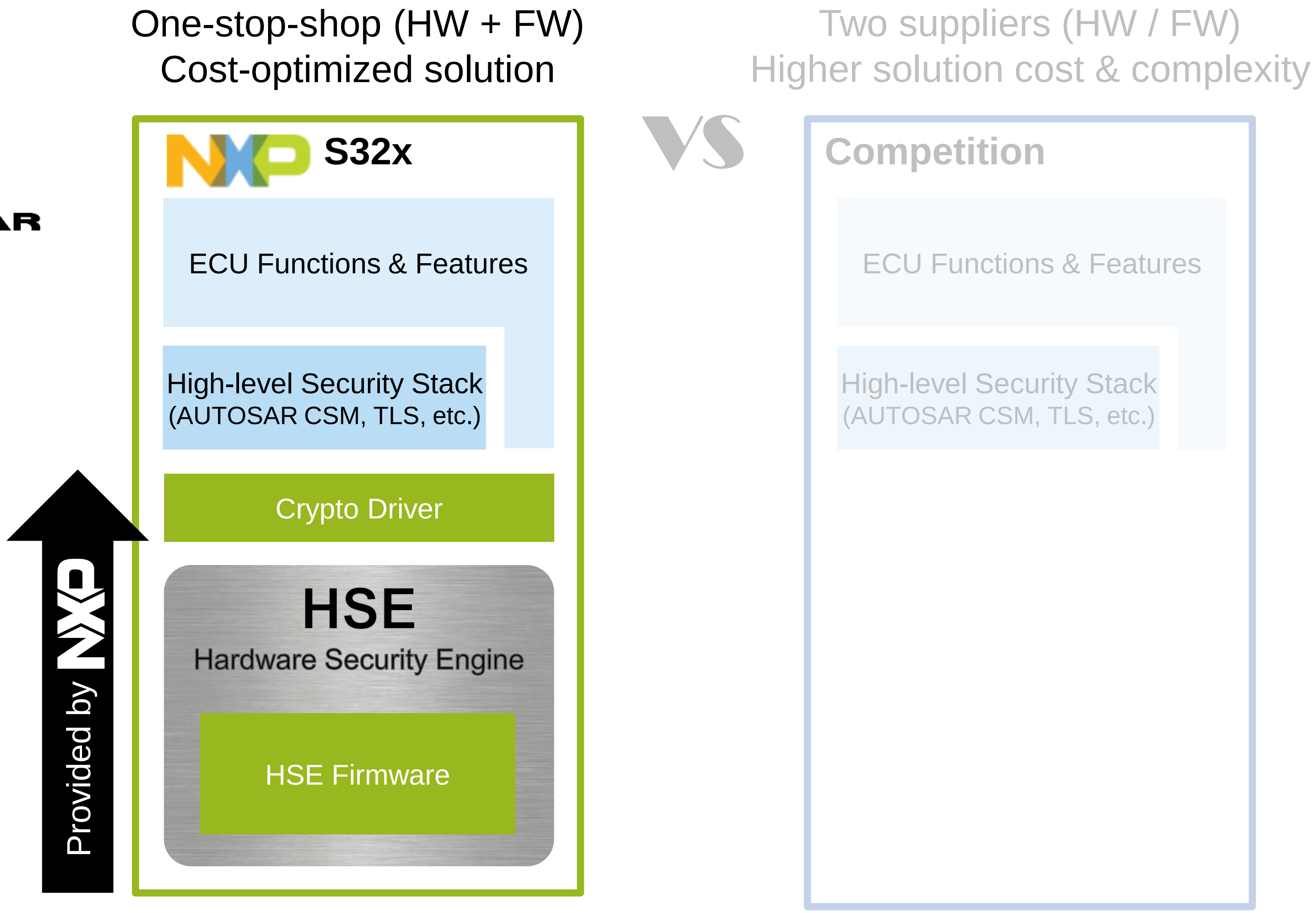

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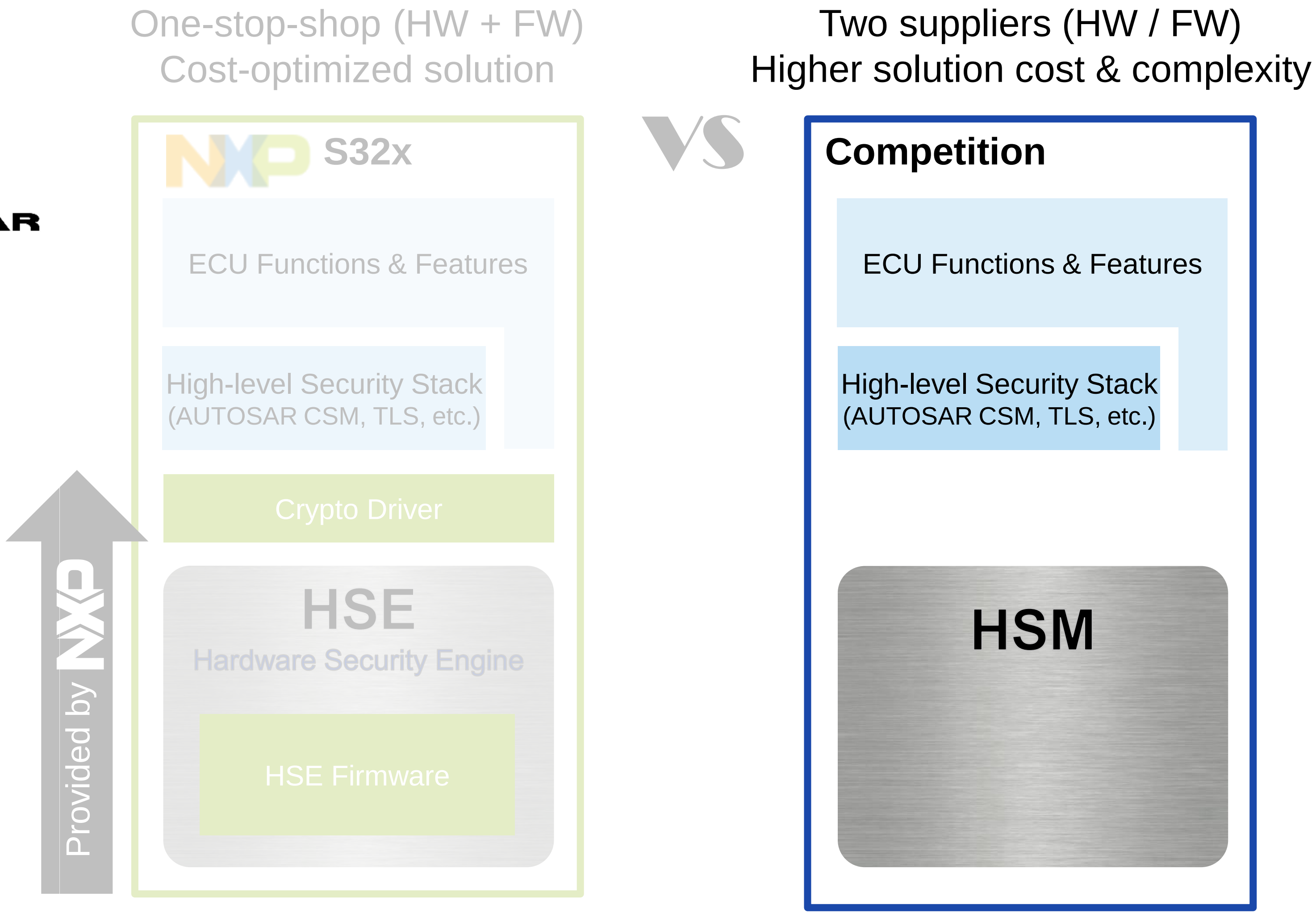

One-stop-shop (HW + FW)
Cost-optimized solution

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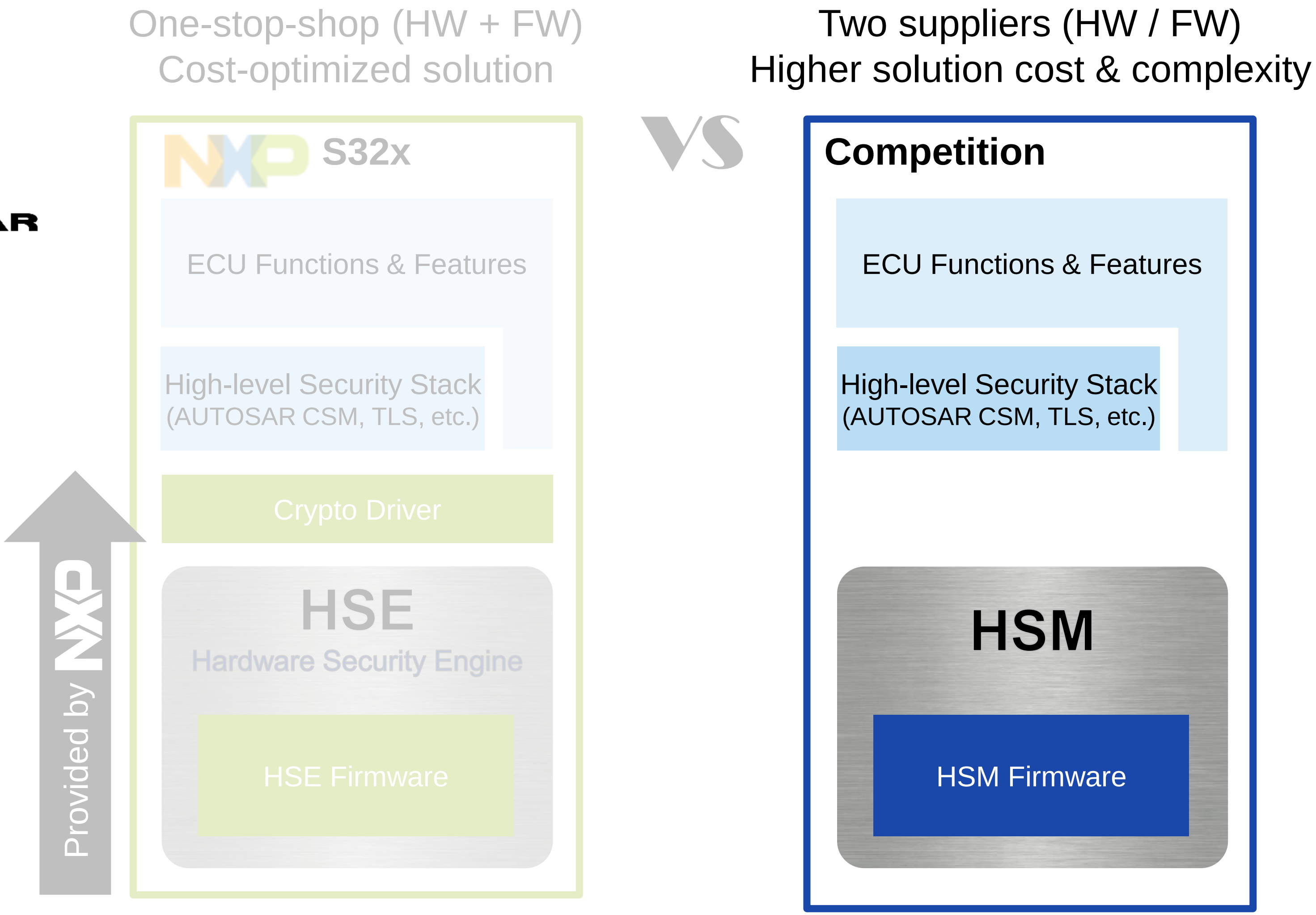

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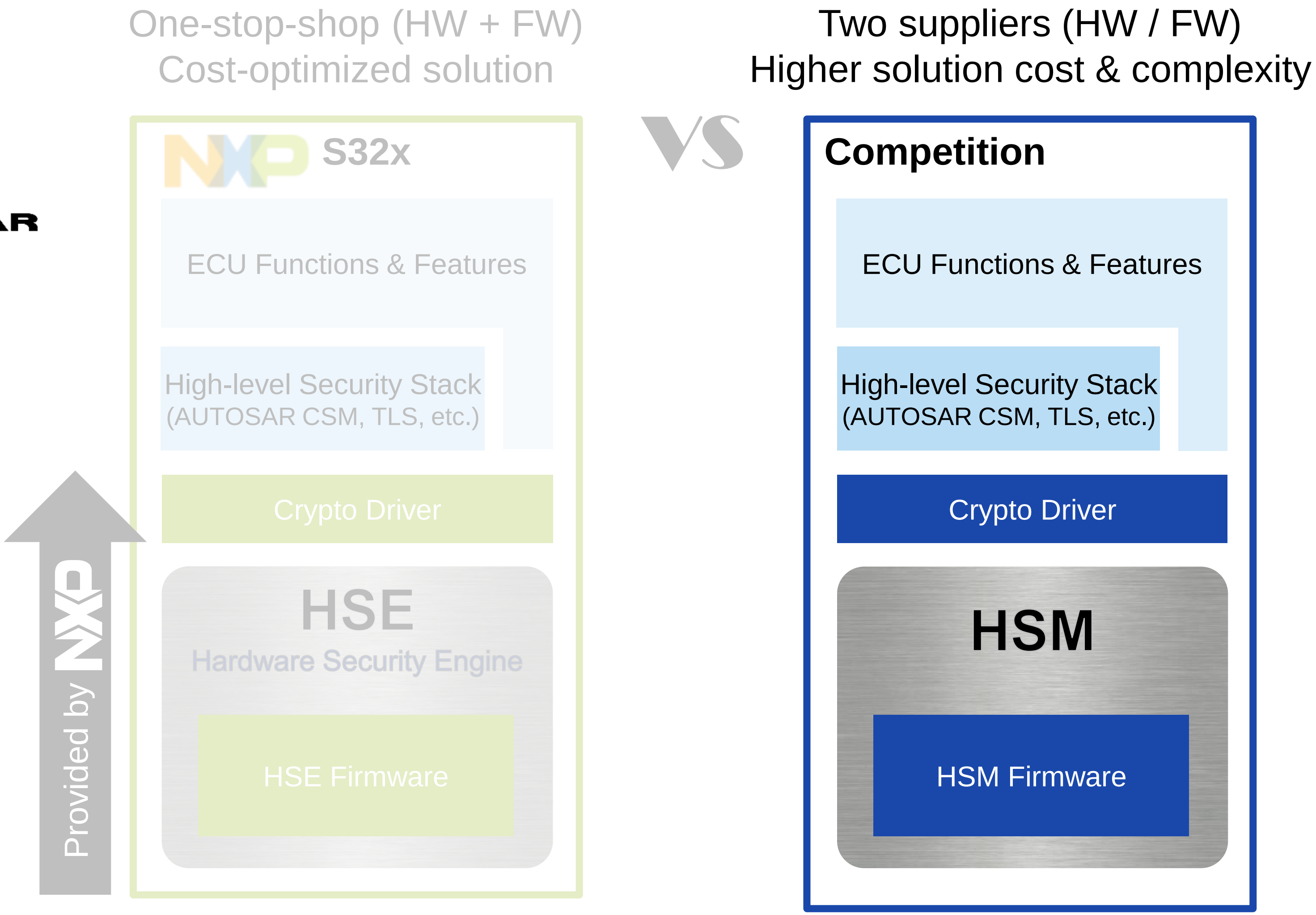

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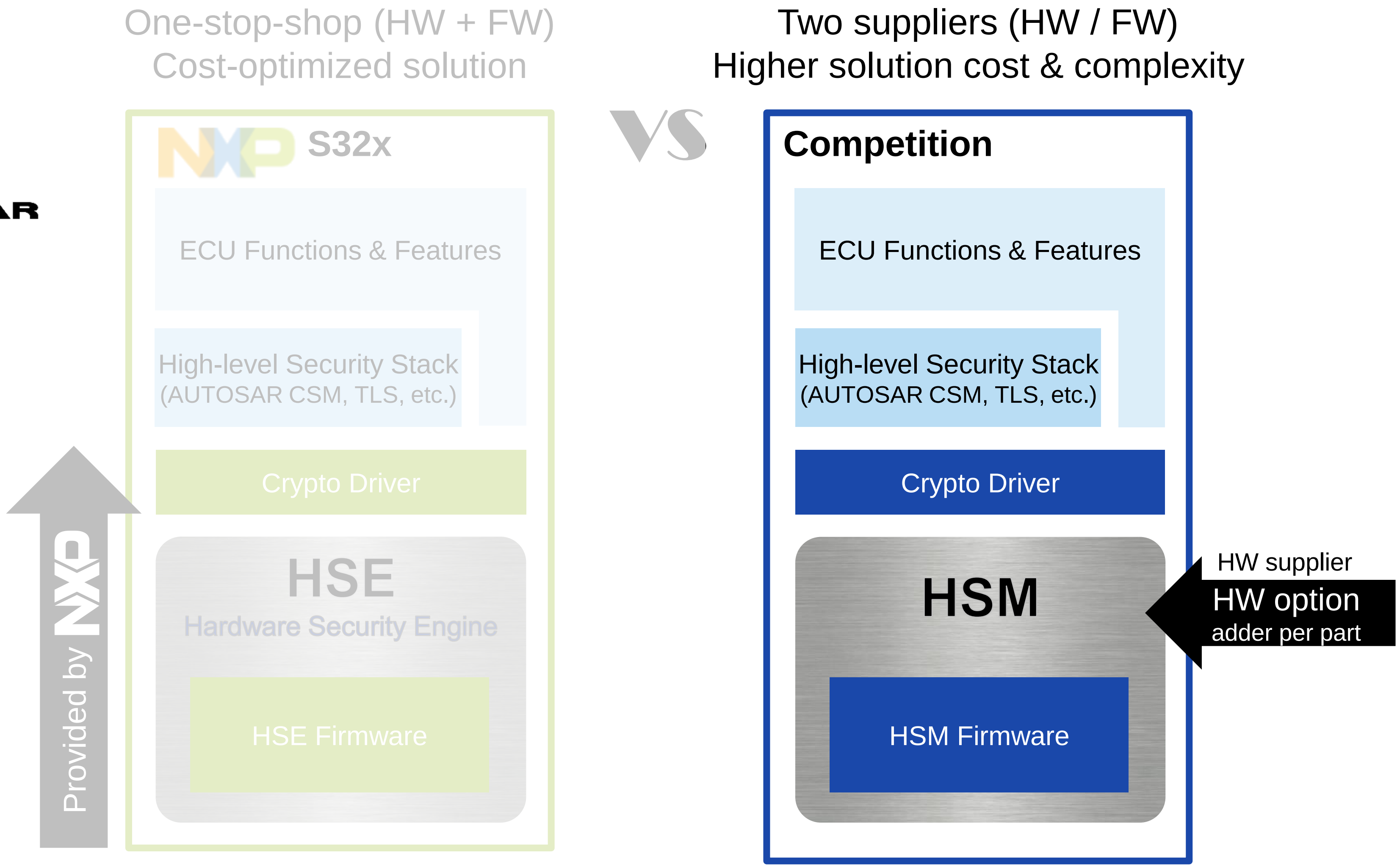

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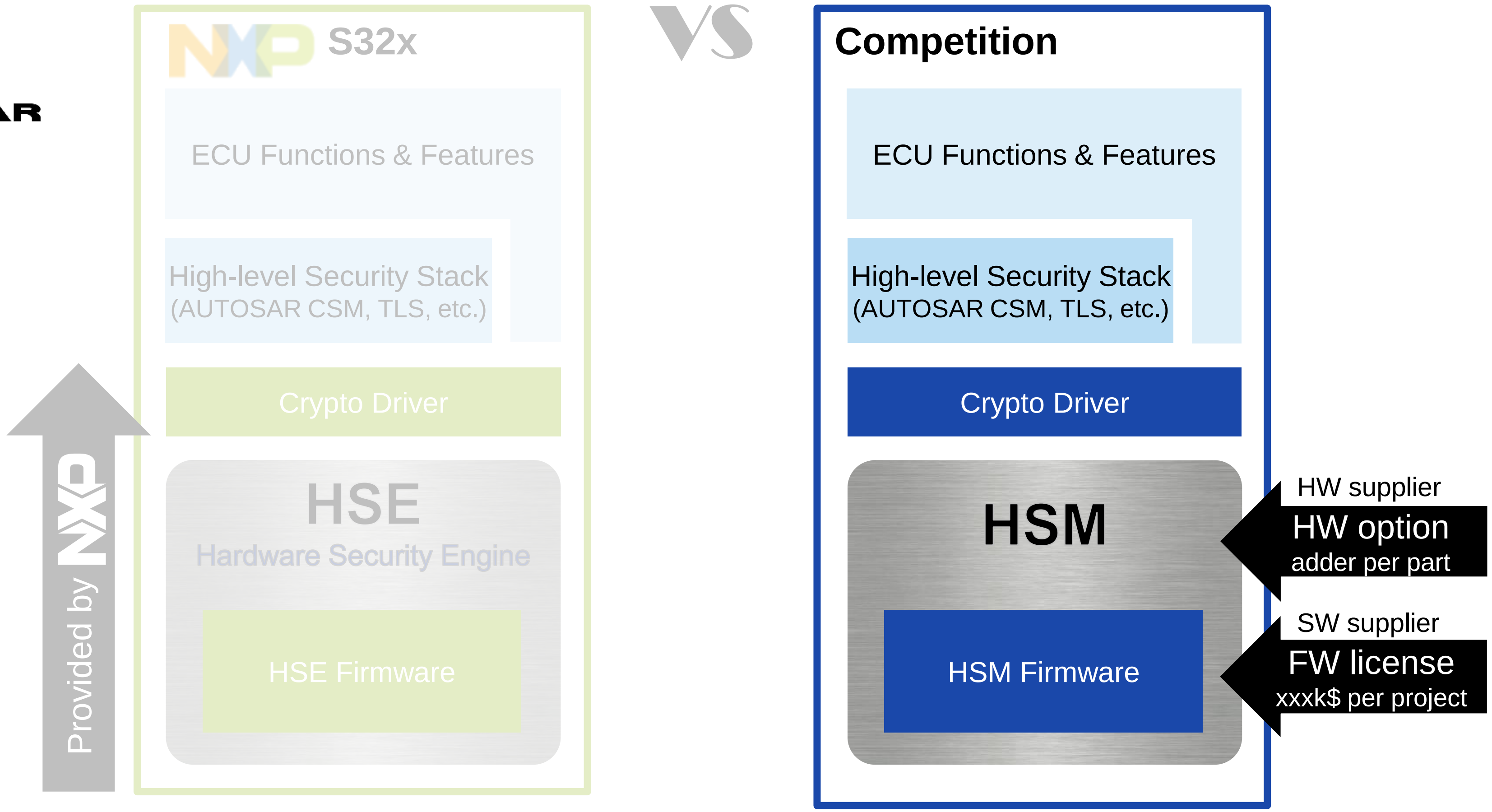

Provided by NXP

NXP S32x

ECU Functions & Features

High-level Security Stack (AUTOSAR CSM, TLS, etc.)

Crypto Driver

HSE
Hardware Security Engine

HSE Firmware

Competition

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HSM

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HW supplier
HW option
adder per part

SW supplier
FW license
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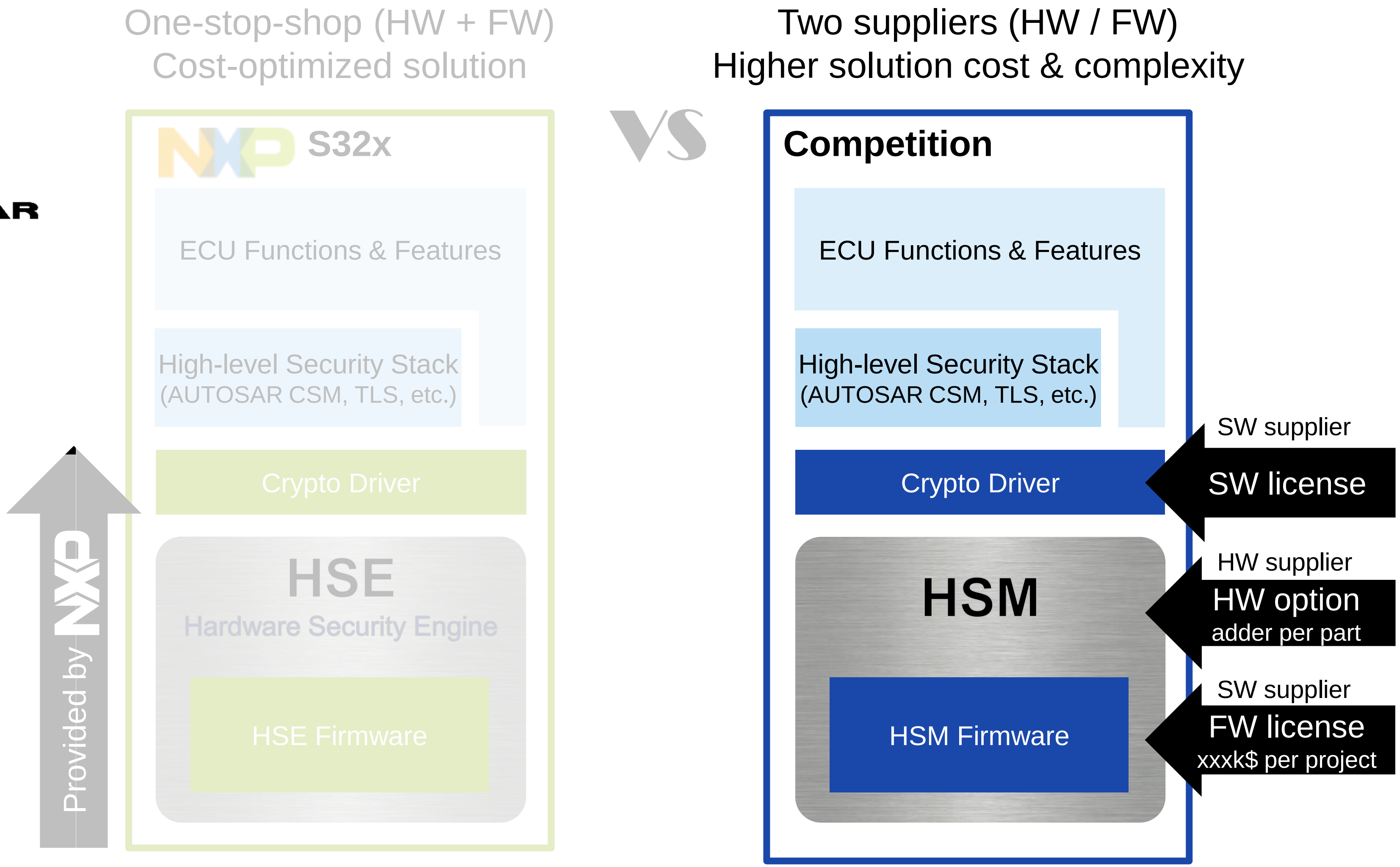

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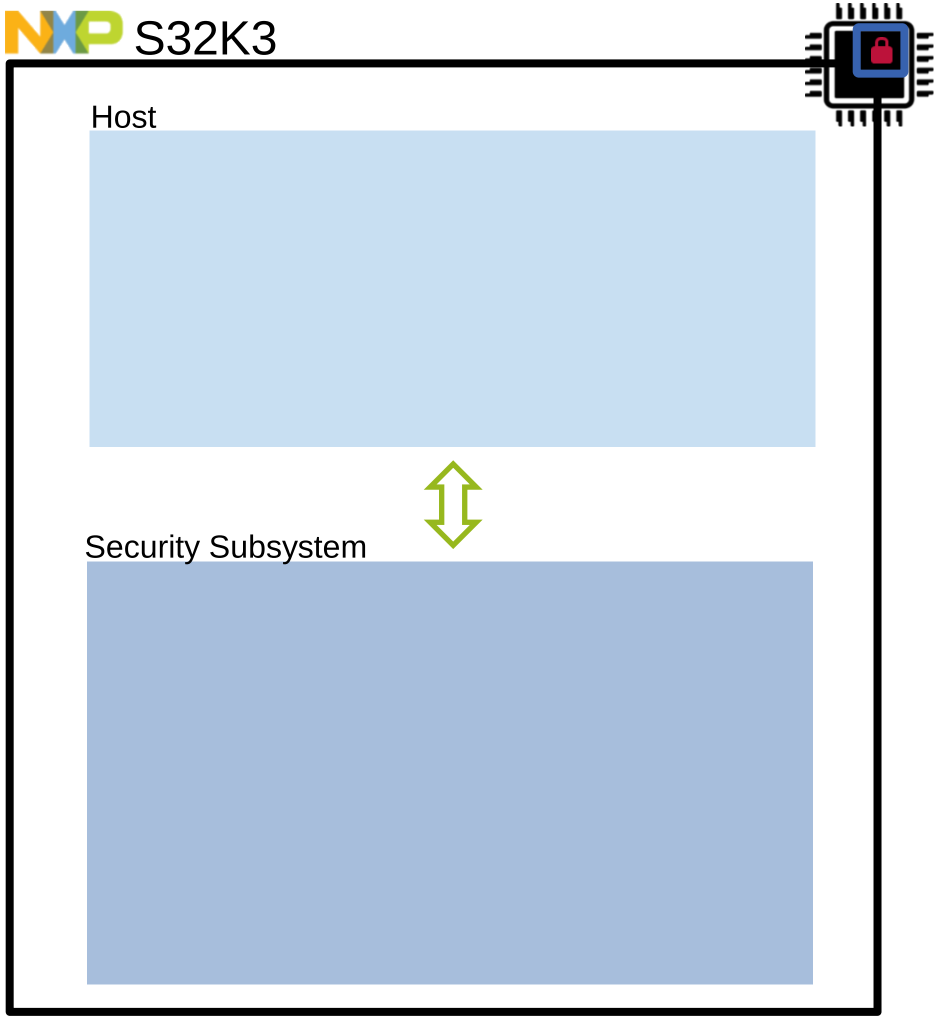
HOW S32K3 SUPPORTS AUTOMOTIVE REQUIREMENTS

SHE

Requirements



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« EVITA-Full »

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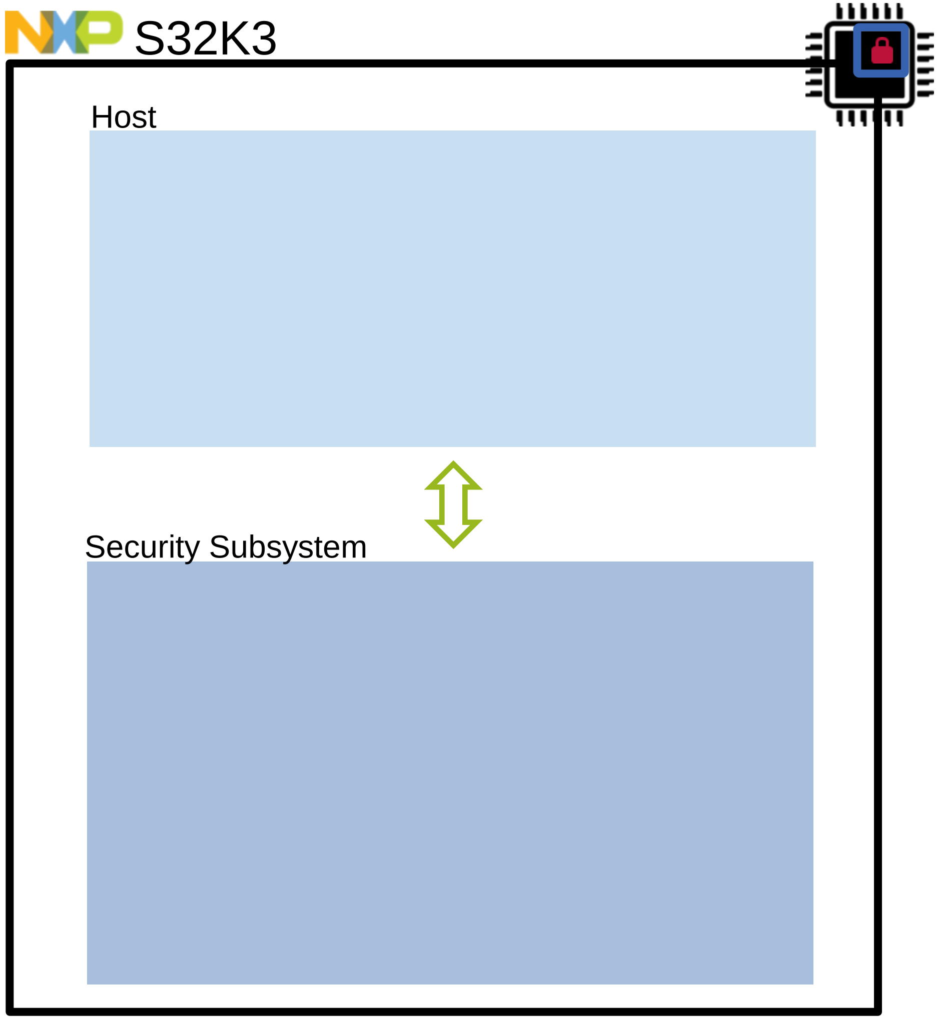

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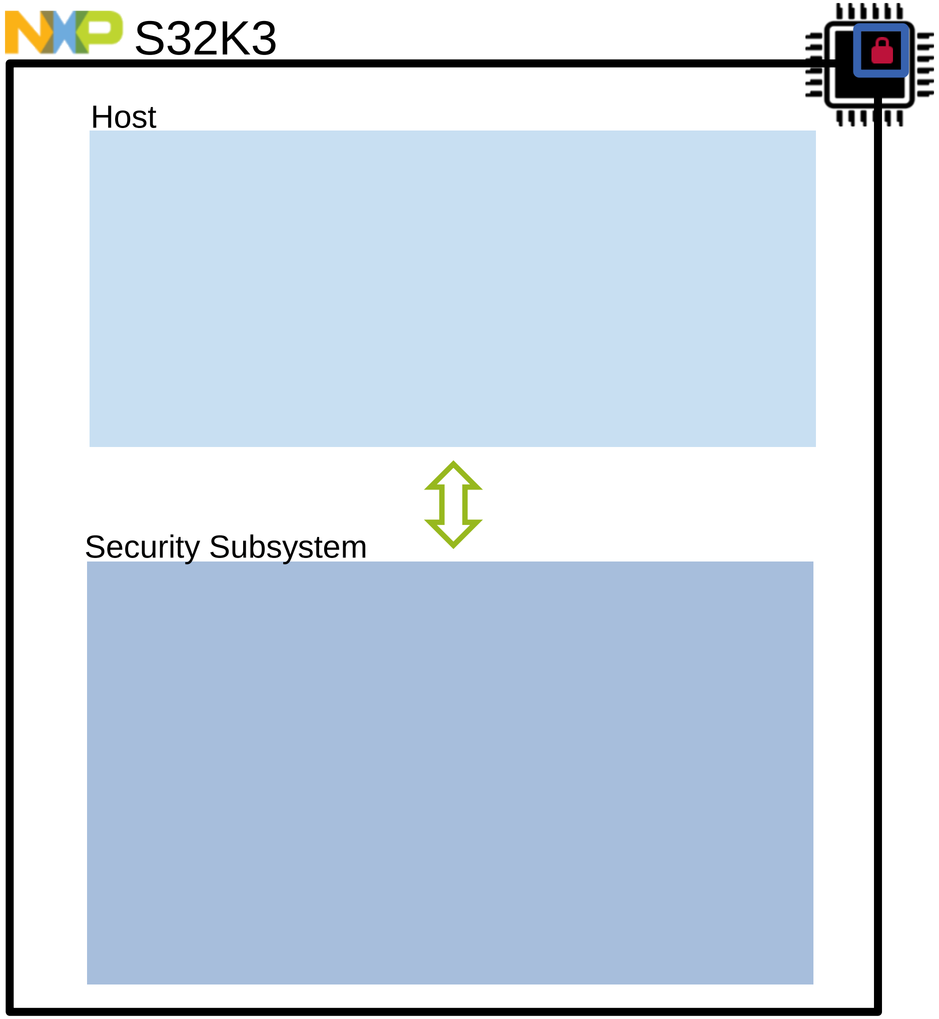

S32K3

Host

Security Subsystem

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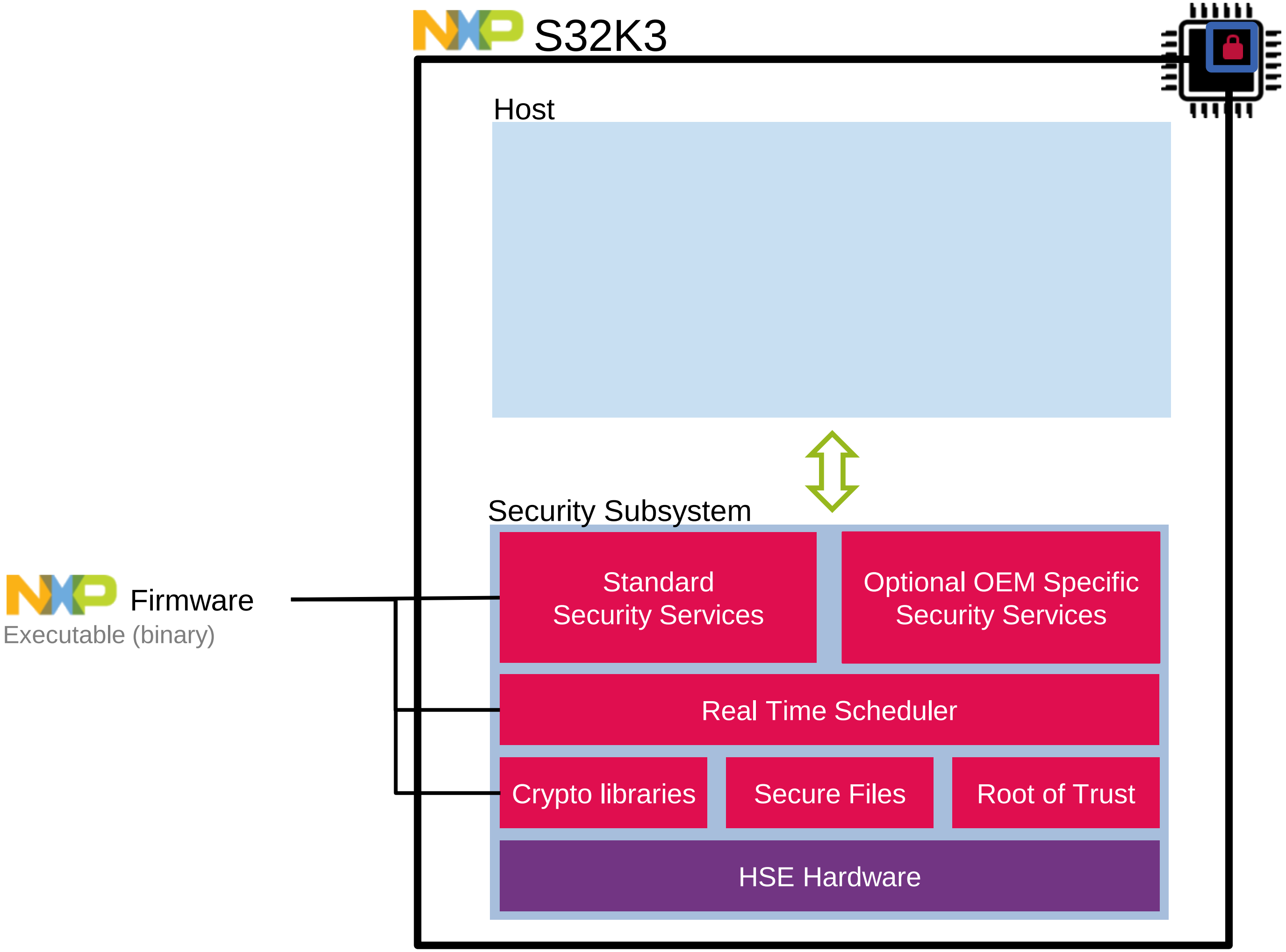

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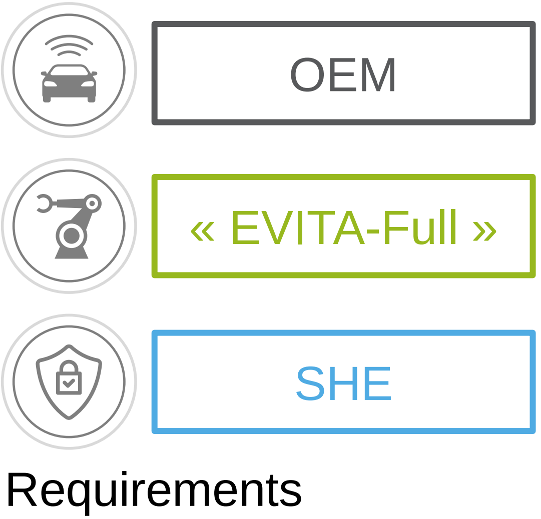

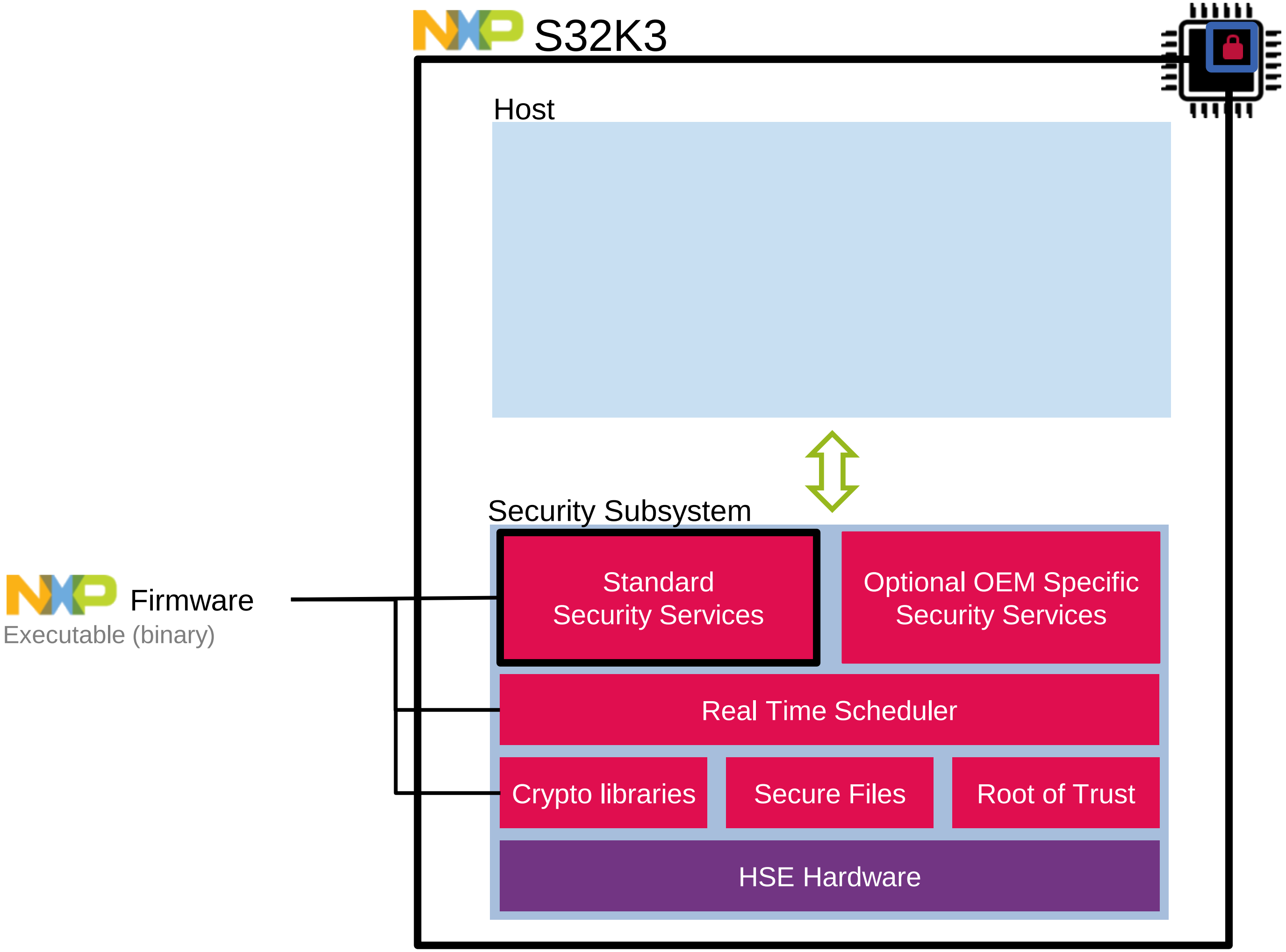

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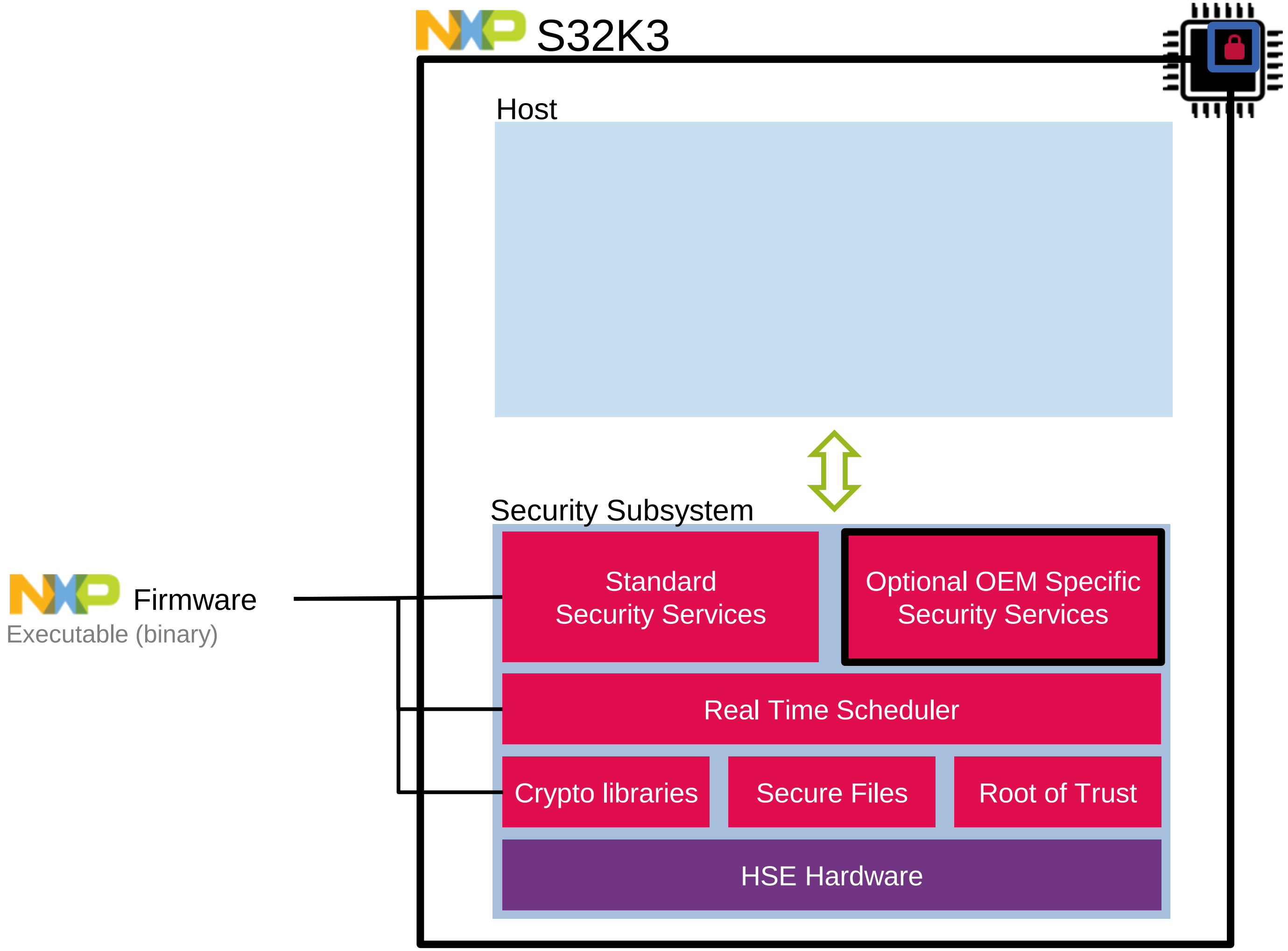

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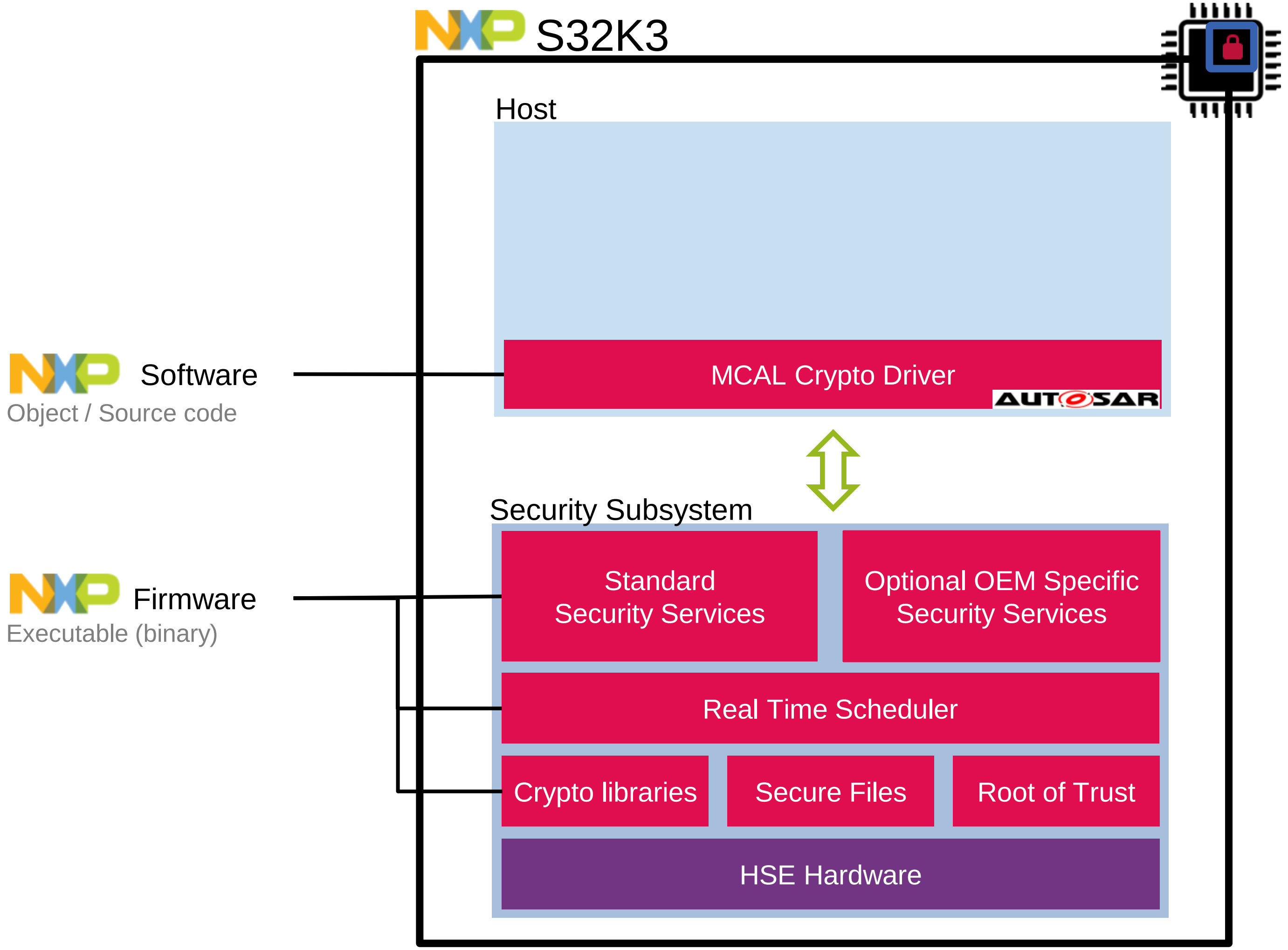
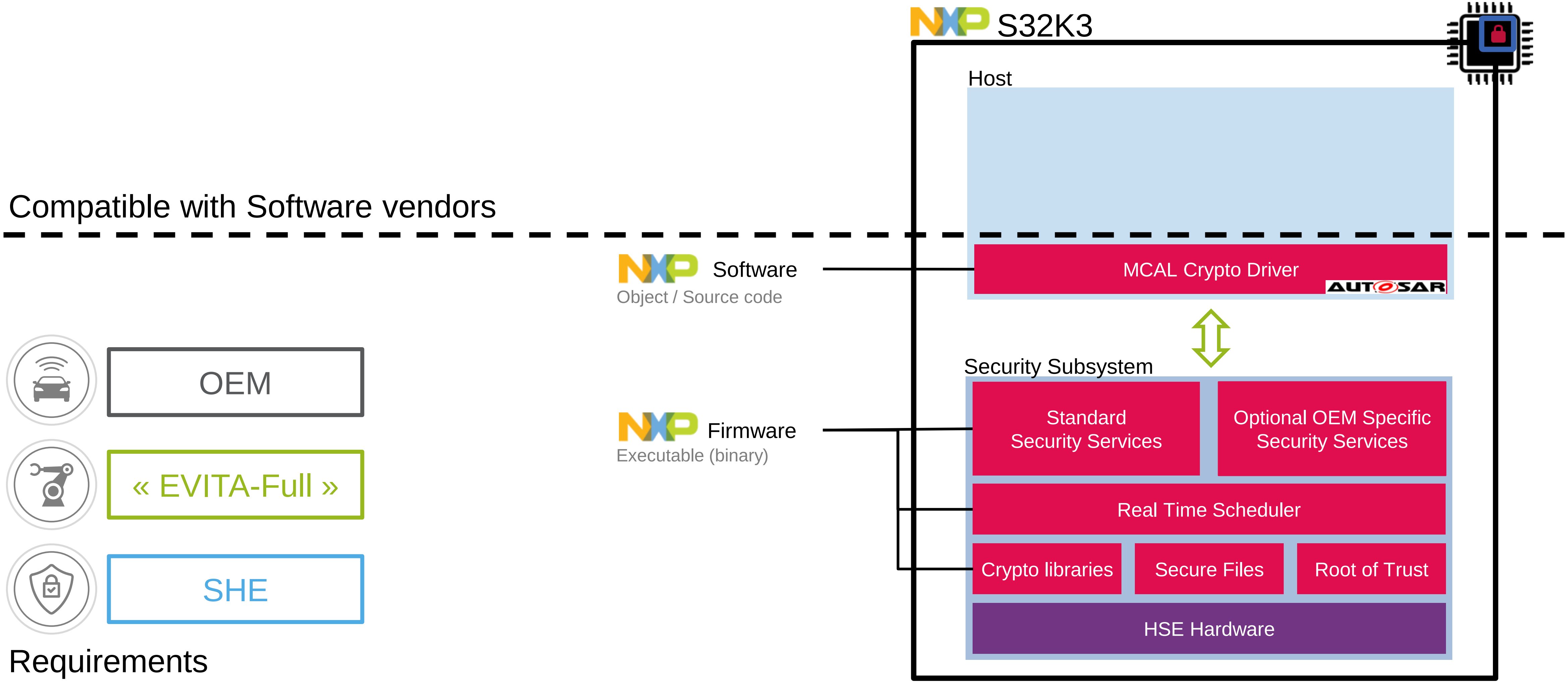


HOW S32K3 SUPPORTS AUTOMOTIVE REQUIREMENTS

Compatible with Software vendors



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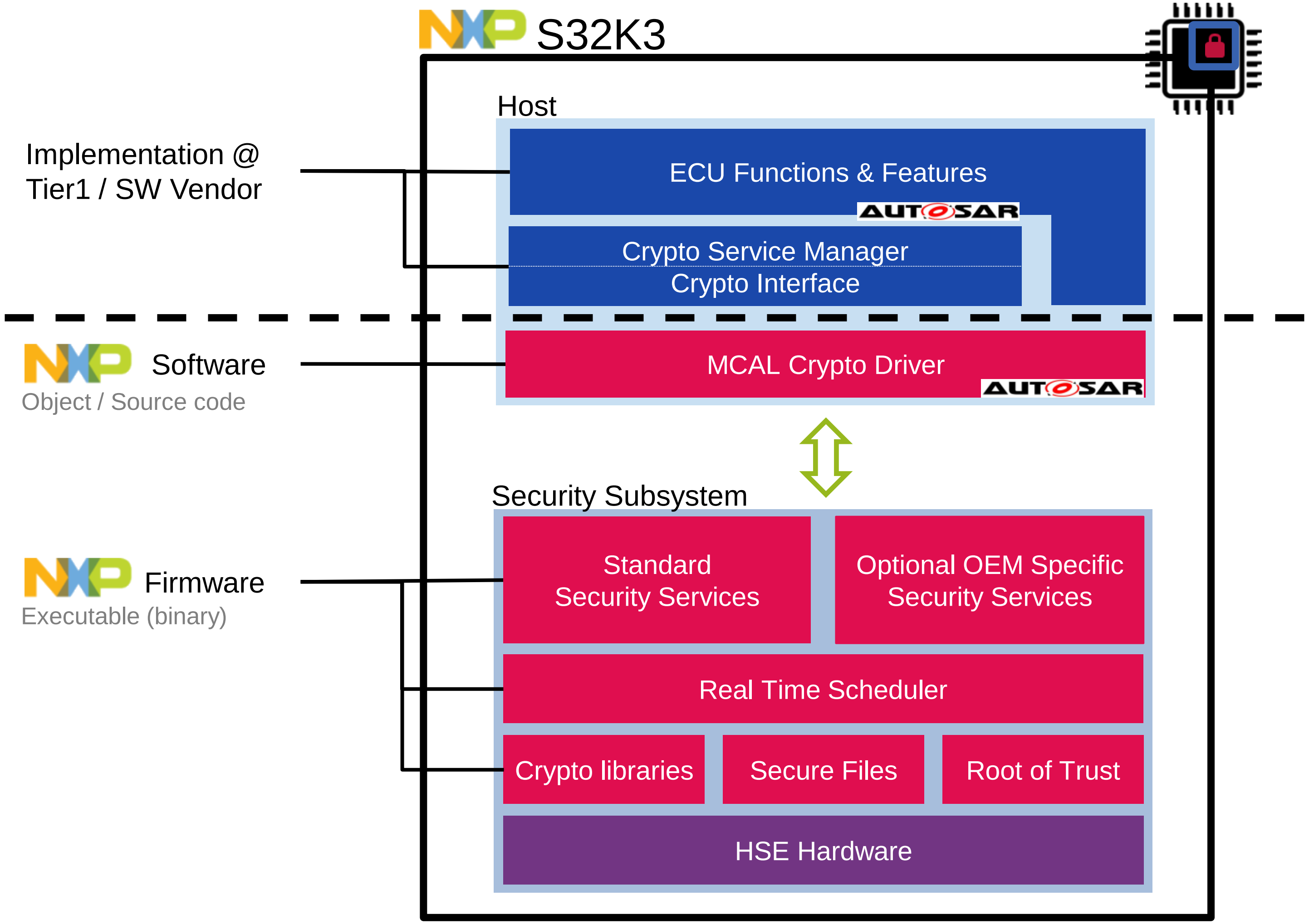

ON-CHIP SECURE SUBSYSTEM: HSE SERVICE EXAMPLES

KEY MANAGEMENT

- Key file management
- Key import
- Key export
- Key generation
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AES key up to 256 bits
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PLATFORM SECURITY

- Strict secure boot
  Verify-then-start
- Parallel secure boot
  Verify-and-start
- On-demand verification
  Secure boot control in app.
- Configurable sanctions
  E.g. key usage restrictions

Secure boot
optimized for latency

NXP: SECURITY 1 STOP-SHOP

- HW, FW and SW co developed and co verified by NXP :
  - **Total quality**
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- Logistics, ECU and Car Manufacturing, In-Field support:
  - Dealing with 1 supplier only, that will manage HW **and** SW issues
  - Cost efficient and streamline solution (no license fee or maintenance for third party FW)

EDGELOCK™ ASSURANCE by NXP

THE S32K3 MICROCONTROLLER WILL BE PART OF THE EDGELOCK™ ASSURANCE PROGRAM

- Provides root-of-trust and implements secure boot, secure debug, lifecycle management, run-time integrity protection
- Features a security enclave (subsystem) that provides security services to the application(s)
- Provides logical and physical isolation of critical assets including crypto keys
- Provides resistance against software attacks and basic hardware attacks such as glitching and basic SCA.
- Security verified and validated under NXP’s secure development process (Security Maturity Process)
- Protection against basic hardware attacks has been assessed and confirmed by NXP’s vulnerability analysis (VA) lab.
- Experienced product support incident response team (PSIRT), and proven process, to professionally handle incidents, if they happen.
- Designed to comply with the ISO/SAE 21434 standard (cybersecurity engineering for road vehicles)

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- Future proof with updatable secure software
- For more information visit nxp.com/S32K3

Q&A

SECURE CONNECTIONS
FOR A SMARTER WORLD

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